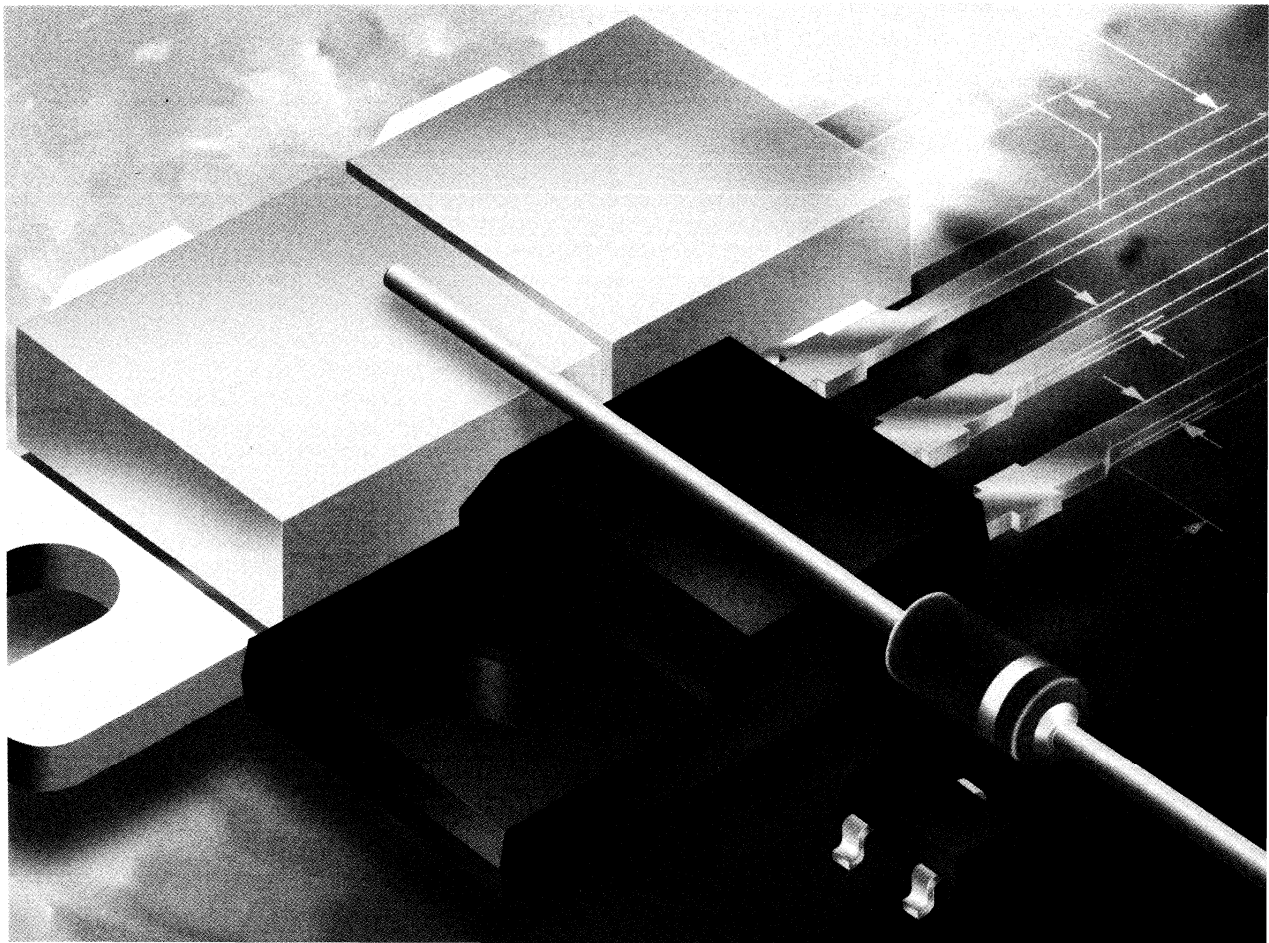


**DISCRETE SEMICONDUCTORS**

# *Discrete Semiconductor Packages*



**1997**

**Data Handbook SC18**

Philips  
Semiconductors



*Let's make things better.*

**PHILIPS**

## **QUALITY ASSURED**

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

## **PRODUCT SAFETY**

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

# Preface

## TABLE OF CONTENTS

<b>Introduction</b> .....	<b>.iii</b>
<b>Chapter 1 - Package overview</b> .....	<b>.1-1</b>
Packages in ascending order of SOD/SOT numbers .....	.1-1
Cross-reference from JEDEC to SOD/SOT .....	.1-21
Cross-reference from EIAJ to SOD/SOT .....	.1-21
<b>Chapter 2 - Package outlines</b> .....	<b>.2-1</b>
<b>Chapter 3 - Handling precautions</b> .....	<b>.3-1</b>
Electrostatic charges .....	.3-1
Workstation for handling electrostatic-sensitive devices .....	.3-1
PCB assembly .....	.3-1
Testing PCBs .....	.3-1
<b>Chapter 4 - Soldering guidelines and SMD footprint design</b> .....	<b>.4-1</b>
Introduction .....	.4-1
Axial and radial devices .....	.4-1
Surface-mount devices .....	.4-2
Recommended footprints .....	.4-13
<b>Chapter 5 - Thermal considerations</b> .....	<b>.5-1</b>
Introduction .....	.5-1
Part one: Thermal properties .....	.5-1
Part two: Worked examples .....	.5-6
Part three: Heat dissipation .....	.5-14
<b>Chapter 6 - Packing methods</b> .....	<b>.6-1</b>
Introduction .....	.6-1
Glossary of terms .....	.6-1
Packing methods in exploded view .....	.6-2
Packing quantities, box dimensions and carrier shapes .....	.6-12

## Preface

---

<b>Chapter 7 - Chemical content of devices</b> .....	<b>7-1</b>
Introduction .....	7-1
Explanation of the tables .....	7-1
Substances not used by Philips Semiconductors .....	7-4
Disposal .....	7-5
Recycling .....	7-5
General warnings .....	7-5
<b>Chapter 8 - Data handbook system</b> .....	<b>8-1</b>

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## Preface

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### INTRODUCTION

Philips Semiconductors is one of the world's leading suppliers of discretes. Our range stretches from small-signal diodes and transistors, through FET power-devices and power rectifiers and triacs, to RF and microwave devices and modules. Such a diverse range of devices requires an equally diverse range of package designs. These packages must not only protect the enclosed circuit and connect it to the outside world, but must also ensure the device operates at its optimum performance in a wide variety of applications.

The discrete semiconductor package, which for many years was only an afterthought in the design and manufacture of electronic systems, increasingly is being recognized as a critical factor in both cost and performance. Indeed, in many applications, the package is often as important as the circuit it encapsulates. And as the functional density of devices and systems increases, the role of the discrete semiconductor package and its interconnections becomes ever more important.

With this in mind, this publication consolidates for the first time, all relevant data for Philips Semiconductors discrete packages in one book – from dimensional outline drawings and soldering information, to thermal design considerations, packing data, and chemical content tables. It should be viewed as a logical extension to our Discrete Semiconductor Data Handbook series and, as such, is intended to serve as a practical data reference to all those involved in production and engineering design, as well as a guide to package selection and availability.

#### An innovative partner

The development of discrete semiconductor packages is a dynamic technology as new and improved circuit processes become available. Applications that until only a few years ago were unattainable, are today common place. From mobile telecommunications and satellite broadcasting to aerospace and automotive applications, each imposes its own individual demands on the electronic package.

To meet these, and future demands, it is essential that the component manufacturer has an intimate knowledge of the multidisciplinary technologies involved to bring the circuit and package together in an optimum design.

Here at Philips, we have been involved in discrete semiconductor package design and development since the early 1950's, during which time we have built up a wealth of experience and know-how in advanced process technologies and assembly procedures. By fully exploiting this expertise, and establishing close working partnerships with our customers, we have developed many market-driven and innovative package designs.

#### How this book is organized

We organized this databook into the following chapters:

**Chapter 1** gives an overview of our discrete semiconductor packages along with a 3-dimensional illustration of each type. Packages are listed in ascending order of Philips outline code and followed by cross-reference lists from the JEDEC and EIAJ numbers to the equivalent Philips SOD/SOT number, where applicable.

**Chapter 2** contains outline dimensional drawings for most of our discrete packages.

**Chapter 3** reviews discrete package handling precautions with emphasis on ESD awareness at the assembly workstation.

**Chapter 4** covers through-hole and SMD soldering and mounting techniques, and includes recommended footprint designs for many SMD packages.

**Chapter 5** is divided into three parts covering: essential thermal properties of discrete semiconductors, worked examples of junction temperatures, and component heat dissipation and heatsink design.

**Chapter 6** contains a survey of some of the packing methods most frequently used and includes the dimensions and shapes of the packing boxes and reels as well as their packing quantities.

**Chapter 7** provides comprehensive data on the chemical composition of our discrete devices with information on their disposal and safety.





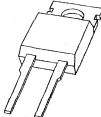



## Package overview

## Chapter 1

### PACKAGE OVERVIEW




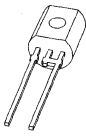
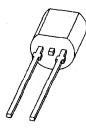

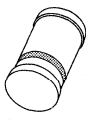

The following table lists our discrete packages in ascending order, and includes a brief description of the package, its 3-dimensional view and the page number on which you'll find the outline drawing. Cross-reference tables from the JEDEC and EIAJ numbers to the equivalent SOD/SOT numbers, where applicable, are given on page 1-21.

### PACKAGES IN ASCENDING ORDER OF SOD/SOT NUMBERS

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOD27	Hermetically sealed glass package; axial leaded; 2 leads		2 - 1
SOD57	Hermetically sealed glass package; axial leaded; 2 leads		2 - 1
SOD59	Plastic single-ended package; heatsink mounted; 1 mounting hole; 2 leads		2 - 2
SOD61A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 3
SOD61AB to AK	Hermetically sealed glass package; axial leaded; 2 leads		2 - 4
SOD61H2	Miniature hermetically sealed glass package; axial leaded; 2 leads		2 - 5

## Package overview








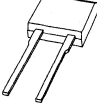
## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOD64	Hermetically sealed glass package; axial leaded; 2 leads		2 - 5
SOD66	Hermetically sealed glass package; axial leaded; 2 leads		2 - 6
SOD68	Hermetically sealed glass package; axial leaded; 2 leads		2 - 6
SOD69	Plastic near cylindrical single-ended package; 2 in-line leads		2 - 7
SOD70	Plastic near cylindrical single-ended package; 2 in-line leads		2 - 8
SOD80	Hermetically sealed glass surface mounted package; 2 connections of contacts		2 - 9
SOD80C	Hermetically sealed glass surface mounted package; 2 connections of contacts		2 - 9
SOD81	Hermetically sealed glass package; cavity free; Implotec™(1) technology; axial leaded; 2 leads		2 - 10



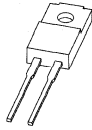

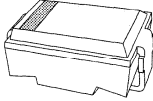

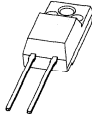
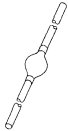

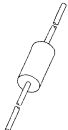
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOD83A	Hermetically sealed glass surface mounted package; 2 connections of contacts		2 - 10
SOD87	Hermetically sealed glass surface mounted package; 2 connections of contacts; Implotec™(1) technology		2 - 11
SOD88A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 11
SOD88B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 12
SOD89A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 12
SOD89B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 13
SOD91	Hermetically sealed glass package; Implotec™(1) technology; axial leaded; 2 leads		2 - 13
SOD95	Plastic single-ended package; 2-lead low-profile		2 - 14

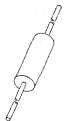
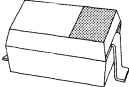
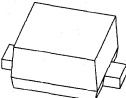





## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOD100	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-lead TO-220F exposed tabs		2 - 15
SOD103	Lacquered glass single-ended package; 2 in-line leads		2 - 16
SOD106	Transfer-moulded thermo-setting plastic small rectangular surface mounted package; 2 connectors		2 - 17
SOD110	Very small ceramic rectangular surface mounted package		2 - 18
SOD113	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-leads TO-220 'full pack'		2 - 19
SOD115	Hermetically sealed glass package; axial leaded; 2 leads		2 - 20
SOD116A to AK	Hermetically sealed glass package; axial leaded; 2 leads		2 - 21
SOD118A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 22

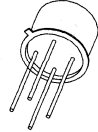
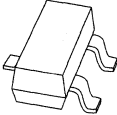
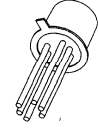
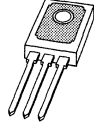
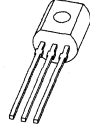
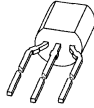
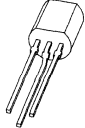
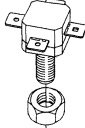
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOD118B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 22
SOD323	Plastic surface mounted package; 2 leads		2 - 23
SOD523	Plastic surface mounted package; 2 leads		2 - 24
SOT5/11	Metal-can cylindrical single-ended package; 3 leads		2 - 25
SOT18/9	Metal-can cylindrical single-ended package; 4 leads		2 - 26
SOT18/13	Metal-can cylindrical single-ended package; 3 leads		2 - 27
SOT18/14	Metal-can cylindrical single-ended package; 4 leads		2 - 28
SOT18/15	Metal-can cylindrical single-ended package; 2 leads		2 - 29

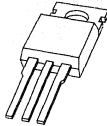
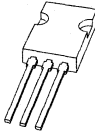
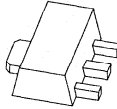
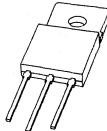
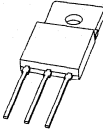
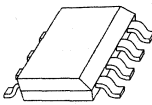
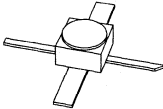
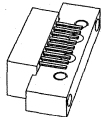
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT18/17	Metal-can cylindrical single-ended package; 4 leads		2 - 30
SOT23	Plastic surface mounted package; 3 leads		2 - 31
SOT31	Metal-can cylindrical single-ended package; 6 leads		2 - 32
SOT32	Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads		2 - 33
SOT54	Plastic single-ended leaded (through hole) package; 3 leads		2 - 34
SOT54A	Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)		2 - 35
SOT54 variant	Plastic single-ended leaded (through hole) package; 3 leads (on-circle)		2 - 36
SOT55E	Studded ceramic package; 4 leads		2 - 37

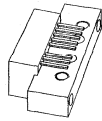
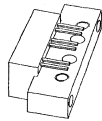
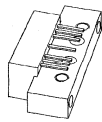
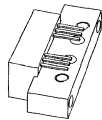
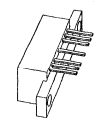
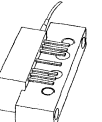
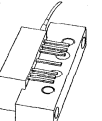
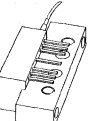
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT78	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead		2 - 38
SOT82	Plastic single-ended package; 3 leads (in-line)		2 - 39
SOT89	Plastic surface mounted package; collector pad for good heat transfer; 3 leads		2 - 40
SOT93A	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)		2 - 41
SOT93B	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)		2 - 42
SOT96-1 (SO8)	Plastic small outline package; 8 leads; body width 3.9 mm		2 - 43
SOT100A	Hermetic ceramic package; 4 leads		2 - 44
SOT115D	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 9 gold-plated in-line leads		2 - 45

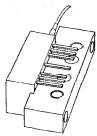
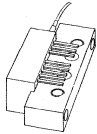
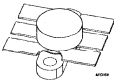
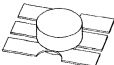
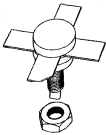
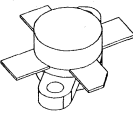
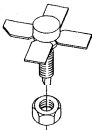
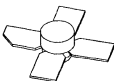
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT115G	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads		2 - 46
SOT115H	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 6 gold-plated in-line leads		2 - 47
SOT115J	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 7 gold-plated in-line leads		2 - 48
SOT115K	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 6 gold-plated in-line leads		2 - 49
SOT115L	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 7 gold-plated in-line leads		2 - 50
SOT115M	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 7 gold-plated in-line leads		2 - 51
SOT115N	Rectangular single-ended flat package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 52
SOT115P	Rectangular single-ended flat package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 53

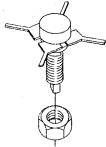
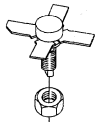
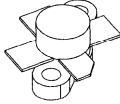
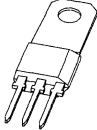
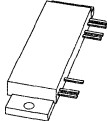
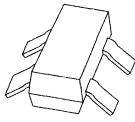
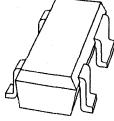
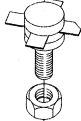
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT115R	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 54
SOT115T	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 8 gold-plated in-line leads		2 - 55
SOT119A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 56
SOT119D	Flangeless ceramic package; 6 leads		2 - 57
SOT120A	Studded ceramic package; 4 leads		2 - 58
SOT121B	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 59
SOT122A	Studded ceramic package; 4 leads		2 - 60
SOT122D	Studless ceramic package; 4 leads		2 - 61

## Package overview

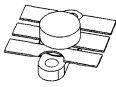
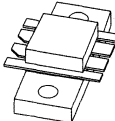
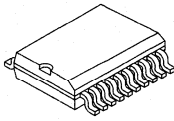
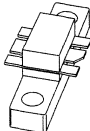
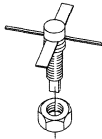
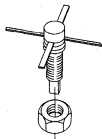
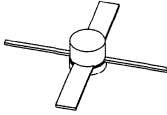
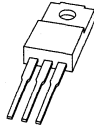
## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT122E	Studded ceramic package; 4 leads		2 - 62
SOT122F	Studded ceramic package; 4 leads		2 - 63
SOT123A	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 64
SOT128B	Plastic single-ended leaded (through hole) package; with cooling fin, mountable to heatsink, 1 mounting hole; 3 leads (in-line)		2 - 65
SOT132B	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 7 in-line leads		2 - 66
SOT143B	Plastic surface mounted package; 4 leads		2 - 67
SOT143R	Plastic surface mounted package; reverse pinning; 4 leads		2 - 68
SOT147A	Studded ceramic package; 4 leads		2 - 69



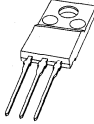

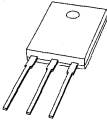
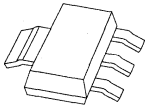
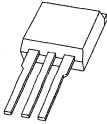
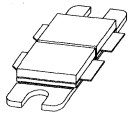
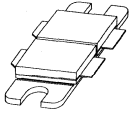
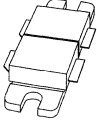
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT160A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 70
SOT161A	Flanged ceramic package; 2 mounting holes; 8 leads		2 - 71
SOT163-1 (SO20)	Plastic small outline package; 20 leads; body width 7.5 mm		2 - 72
SOT171A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 73
SOT172A1	Studded ceramic package; 4 leads		2 - 74
SOT172A2	Studded ceramic package; 4 leads		2 - 75
SOT172D	Studless ceramic package; 4 leads		2 - 76
SOT186	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 exposed tabs		2 - 77

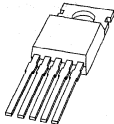
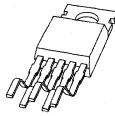
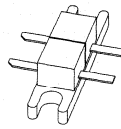
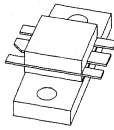
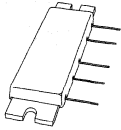
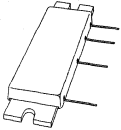
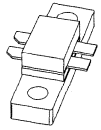
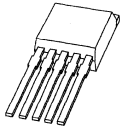
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT186A	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead		2 - 78
SOT195	Plastic single-ended flat package; 4 in-line leads		2 - 79
SOT199	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)		2 - 80
SOT223	Plastic surface mounted package; collector pad for good heat transfer; 4 leads		2 - 81
SOT226	Plastic single-ended package; 3 lead low-profile TO-220		2 - 82
SOT262A1	Flanged ceramic package double-ended; 2 mounting holes; 4 leads		2 - 83
SOT262A2	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 84
SOT262B	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 85

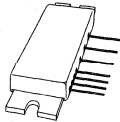
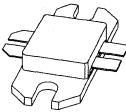
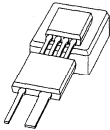
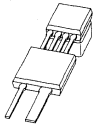
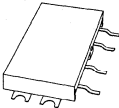
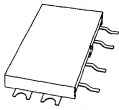
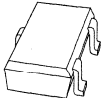
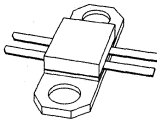
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT263	Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220		2 - 86
SOT263-01	Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220 lead form option		2 - 87
SOT268A	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 88
SOT273A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 89
SOT278A	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 5 in-line leads		2 - 90
SOT278B	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads		2 - 91
SOT279A	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 92
SOT281	Plastic single-ended package; 5-lead low-profile		2 - 93



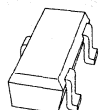
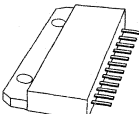
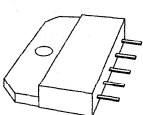
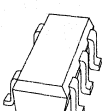
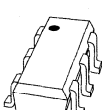

Package overview

Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT288D	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 7 in-line leads		2 - 94
SOT289A	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 95
SOT312A	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8.0 x 8.0 x 4.5 mm); 2 in-line leads		2 - 96
SOT312B	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 4.0 mm); 2 in-line leads		2 - 97
SOT321	Rectangular single-ended surface-mount package; metal cap; flange mounted; 4 in-line leads		2 - 98
SOT321B	Rectangular single-ended surface-mount package; metal cap; flange mounted; 4 in-line leads		2 - 99
SOT323	Plastic surface mounted package; 3 leads		2 - 100
SOT324B	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 101


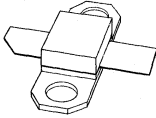
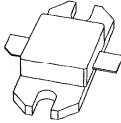
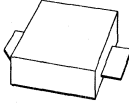
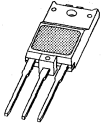
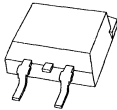
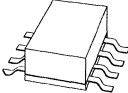
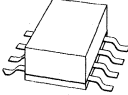
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT343N	Plastic surface mounted package; 4 leads		2 - 102
SOT343R	Plastic surface mounted package; 4 leads		2 - 103
SOT346	Plastic surface mounted package; 3 leads		2 - 104
SOT347	Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads		2 - 105
SOT348	Rectangular single-ended flat package; plastic cap; heatsink mounted; 1 mounting hole; 5 in-line gold-metallized leads		2 - 106
SOT353	Plastic surface mounted package; 5 leads		2 - 107
SOT363	Plastic surface mounted package; 6 leads		2 - 108
SOT365	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads		2 - 109

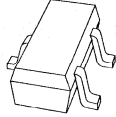

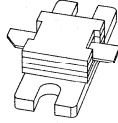
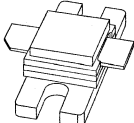
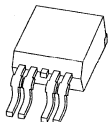
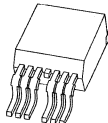
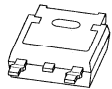
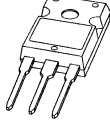
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT388A	Rectangular single-ended surface-mount package; metal cap; 4 in-line leads		2 - 110
SOT390A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 111
SOT391A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 112
SOT391B	Flangeless ceramic package; 2 leads		2 - 113
SOT399	Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads		2 - 114
SOT404	Plastic single-ended package (Philips version of D <sup>2</sup> Pak); 2 leads		2 - 115
SOT409A	Ceramic surface mounted package; 8 leads		2 - 116
SOT409B	Ceramic surface mounted package; 8 leads		2 - 117

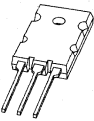
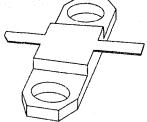
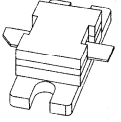
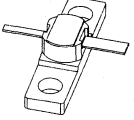
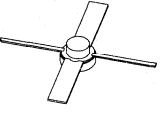
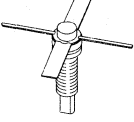
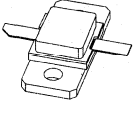
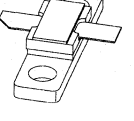
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT416	Plastic surface mounted package; 3 leads		2 - 118
SOT421A	Ceramic single-ended flat package; 4 in-line leads		2 - 119
SOT422A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 120
SOT423A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 121
SOT426	Plastic single-ended package (Philips version of D <sup>2</sup> Pak); 4 leads		2 - 122
SOT427	Plastic single-ended package (Philips version of D <sup>2</sup> Pak); 6 leads		2 - 123
SOT428	Plastic surface mounted package (Philips version of DPak); 2 leads		2 - 124
SOT429	Plastic single-ended flat package; heatsink mounted; 1 mounting hole; 3 leads		2 - 125

## Package overview



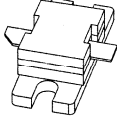
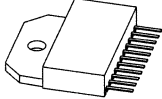
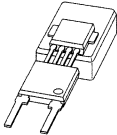
## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT430	Plastic single-ended flat package; heatsink mounted; 1 mounting hole; 3 leaded JUMBO TO-247		2 - 126
SOT437A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 127
SOT439A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 128
SOT440A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 129
SOT441A	Studless ceramic package; 4 leads		2 - 130
SOT442A	Studded ceramic package; 4 leads		2 - 131
SOT443A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 132
SOT445A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 133



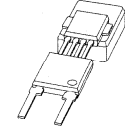
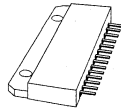
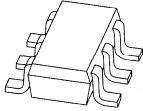
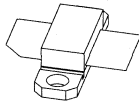
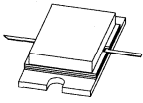
## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT445B	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 134
SOT445C	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 135
SOT446A	Studless hermetic ceramic package; 2 leads		2 - 136
SOT447A	Flangeless ceramic package; 2 leads		2 - 137
SOT448A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 138
SOT451A	Ceramic single-ended flat package; heatsink mounted; 1 mounting hole; 11 in-line gold-metallized leads		2 - 139
SOT453A	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (3.8 x 2.0 x 0.8 mm); 2 in-line leads		2 - 140
SOT453B	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8.0 x 8.0 x 4.5 mm); 2 in-line leads		2 - 141

## Package overview

## Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (NOT TO SCALE)	PAGE
SOT453C	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 3.0 mm); 2 in-line leads		2 - 142
SOT454A	Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 14 in-line tin (Sn) plated leads		2 - 143
SOT457	Plastic surface mounted package; 6 leads		2 - 144
SOT460A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 145
SOT469A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 146

## Package overview

## Chapter 1

## CROSS-REFERENCE FROM JEDEC TO SOD/SOT

JEDEC	OUTLINE	PAGE
DO-34	SOD68	2 - 6
DO-35	SOD27	2 - 1
DO-41	SOD66	2 - 6
DO-214AC	SOD106	2 - 17
MS-012AA	SOT96-1	2 - 43
MS-013AC	SOT163-1	2 - 72
TO-18	SOT18/13	2 - 27
TO-18	SOT18/15	2 - 29
TO-39	SOT5/11	2 - 25
TO-71	SOT31	2 - 32
TO-72	SOT18/9	2 - 26
TO-72	SOT18/14	2 - 28
TO-72	SOT18/17	2 - 30
TO-92	SOT54	2 - 34
TO-126	SOT32	2 - 33
TO-202AA	SOT128B	2 - 65
TO-220	SOD95	2 - 14
TO-220	SOT226	2 - 82
TO-220	SOT263	2 - 86
TO-220	SOT263-01	2 - 87
TO-220	SOT281	2 - 93
TO-220AB	SOT78	2 - 38
TO-220AC	SOD59	2 - 2
TO-220F	SOD100	2 - 15
TO-220F	SOD113	2 - 19
TO-220F	SOT186	2 - 77
TO-220F	SOT186A	2 - 78
TO-236	SOT346	2 - 104
TO-236AB	SOT23	2 - 31
TO-243	SOT89	2 - 40
TO-247	SOT429	2 - 125

## CROSS-REFERENCE FROM EIAJ TO SOD/SOT

EIAJ	OUTLINE	PAGE
SC-40	SOD27	2 - 1
SC-43	SOT54	2 - 34
SC-46	SOT78	2 - 38
SC-53	SOT128B	2 - 65
SC-59	SOT346	2 - 104
SC-61B	SOT143R	2 - 68
SC-62	SOT89	2 - 40
SC-63	SOT428	2 - 124
SC-67	SOT186	2 - 77
SC-70	SOT323	2 - 100
SC-73	SOT223	2 - 81
SC-74	SOT457	2 - 144
SC-75	SOT416	2 - 118
SC-76	SOD323	2 - 23
SC-79	SOD523	2 - 24
SC-88	SOT363	2 - 108
SC-88A	SOT353	2 - 107



Package outlines

Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads

SOD27

**DIMENSIONS (mm are the original dimensions)**

UNIT	b max.	D max.	G <sub>1</sub> max.	L min.
mm	0.56	1.85	4.25	25.4

0 1 2 mm scale

**Note**  
1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD27	A24	DO-35	SC-40			97-06-09

Hermetically sealed glass package; axial leaded; 2 leads

SOD57

**DIMENSIONS (mm are the original dimensions)**

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.81	4.57	28

0 2.5 5 mm scale

**Note**  
1. The marking band indicates the cathode.

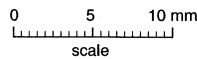
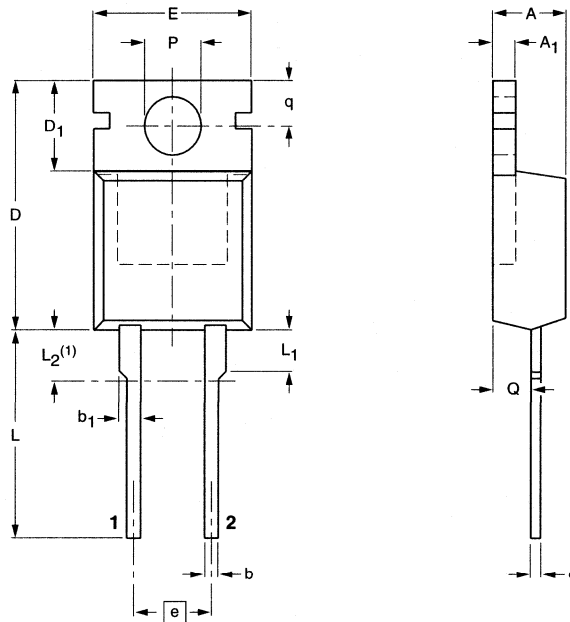
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD57						97-06-09

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 2-lead TO-220

SOD59



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup>	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	5.08	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

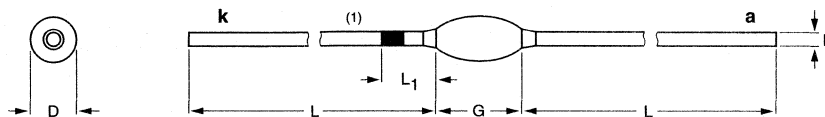
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD59		2-lead TO-220				97-06-11

Package outlines

Chapter 2

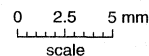
Hermetically sealed glass package; axial leaded; 2 leads

SOD61A



DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.	L <sub>1</sub> max.
mm	0.6	2.5	4.9	32.5	3



Note

- The marking band indicates the cathode.

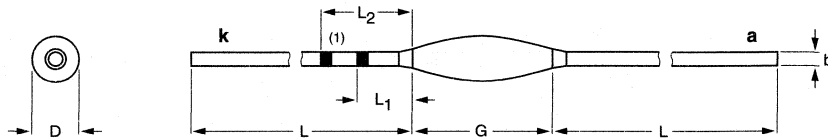
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61A						97-06-09

Package outlines

Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads

SOD61AB to AK



DIMENSIONS (mm are the original dimensions)

OUTLINE VERSION	UNIT	b	D max.	G max.	L min.	L1 max.	L2 max.
SOD61AB	mm	0.6	2.5	5.5	31.8	3	5
SOD61AC	mm	0.6	2.5	8.3	30.4	3	5
SOD61AD	mm	0.6	2.5	8.7	30.2	3	5
SOD61AE	mm	0.6	2.5	9.1	30.0	3	5
SOD61AF	mm	0.6	2.5	9.5	29.8	3	5
SOD61AG	mm	0.6	2.5	9.9	29.6	3	5
SOD61AH	mm	0.6	2.5	10.5	29.3	3	5
SOD61AI	mm	0.6	2.5	11.5	28.8	3	5
SOD61AJ	mm	0.6	2.5	12.5	28.3	3	5
SOD61AK	mm	0.6	2.5	13.5	27.8	3	n.a

Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD61AB to AK					97-06-20

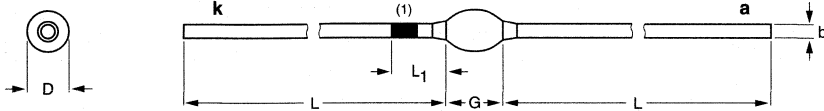


Package outlines

Chapter 2

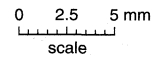
Miniature hermetically sealed glass package; axial leaded; 2 leads

SOD61H2



DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.	L1 max.
mm	0.6	2.2	3	32.5	3



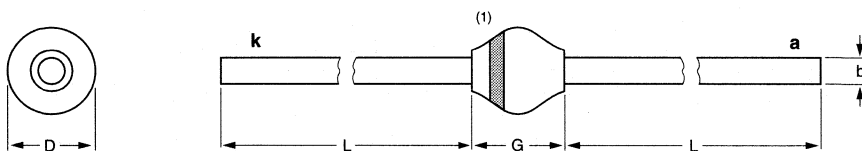
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61H2						97-06-09

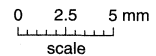
Hermetically sealed glass package; axial leaded; 2 leads

SOD64



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	1.35	4.5	5.0	28



Note

1. The marking band indicates the cathode.

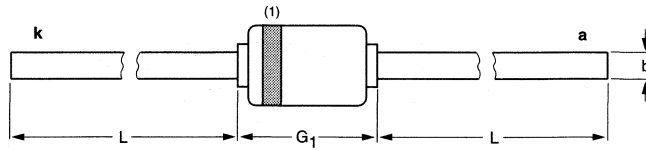
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD64						97-06-09

Package outlines

Chapter 2

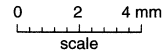
Hermetically sealed glass package; axial leaded; 2 leads

SOD66



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G <sub>1</sub> max.	L min.
mm	0.81	2.6	4.8	28



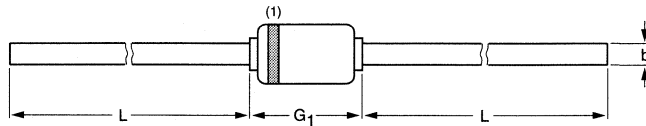
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD66		DO-41			97-06-20

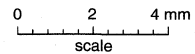
Hermetically sealed glass package; axial leaded; 2 leads

SOD68



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G <sub>1</sub> max.	L min.
mm	0.55	1.6	3.04	25.4



Note

1. The marking band indicates the cathode.

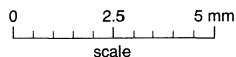
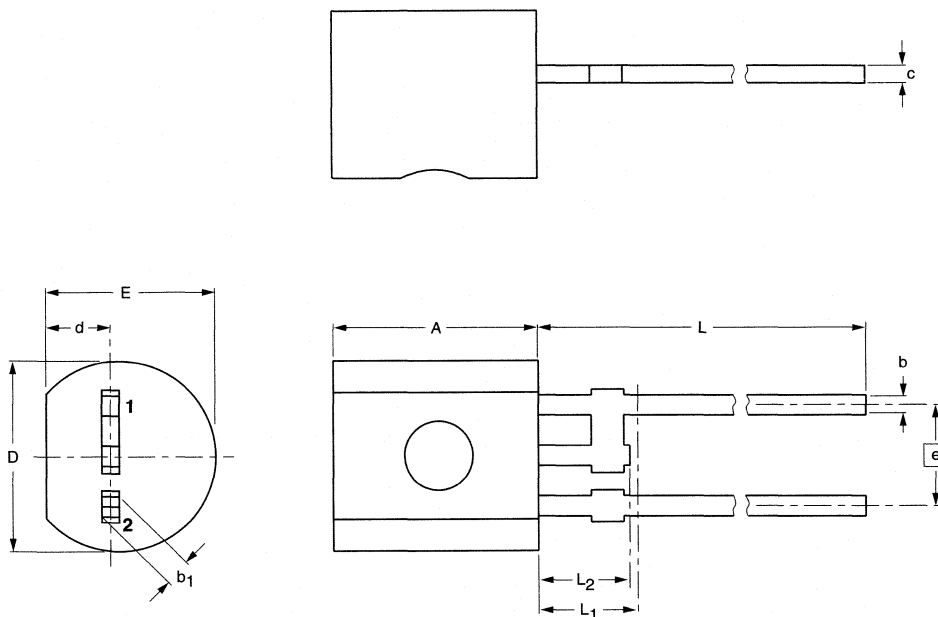
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD68		DO-34			97-06-09

Package outlines

Chapter 2

Plastic near cylindrical single-ended package; 2 in-line leads

SOD69



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	L	L <sub>1</sub> <sup>(1)</sup> max.	L <sub>2</sub>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	14.5 12.7	2.5	2.1 1.9

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

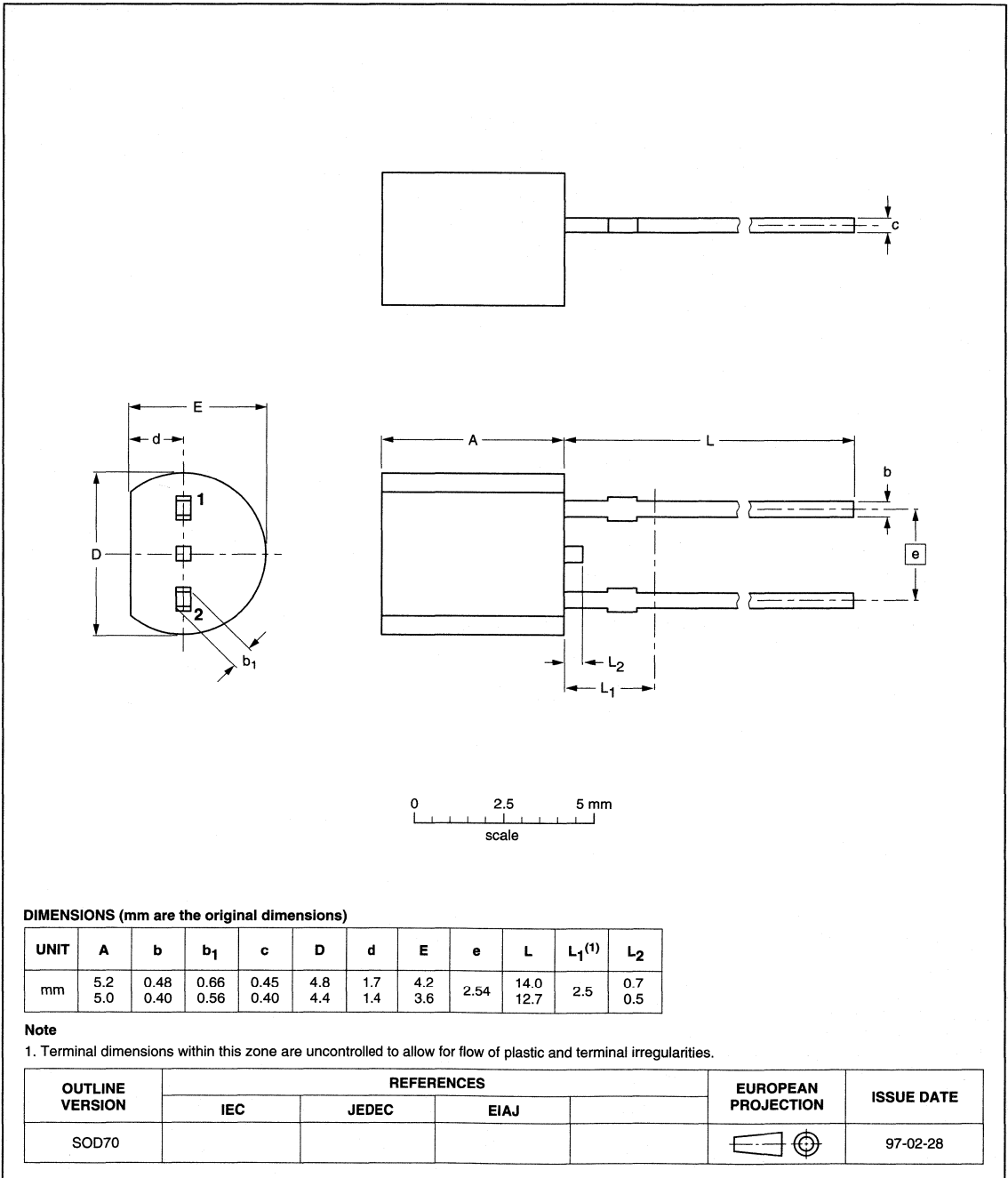
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD69						97-06-02

Package outlines

Chapter 2

Plastic near cylindrical single-ended package; 2 in-line leads

SOD70



Package outlines

Chapter 2

Hermetically sealed glass surface mounted package; 2 connectors

SOD80

**DIMENSIONS (mm are the original dimensions)**

UNIT	D	H	L
mm	1.7 1.5	3.7 3.3	0.3

0 1 2 mm  
scale

**Note**  
1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD80	100H02				97-06-20

Hermetically sealed glass surface mounted package; 2 connectors

SOD80C

**DIMENSIONS (mm are the original dimensions)**

UNIT	D	H	L
mm	1.60 1.45	3.7 3.3	0.3

0 1 2 mm  
scale

**Note**  
1. The marking band indicates the cathode.

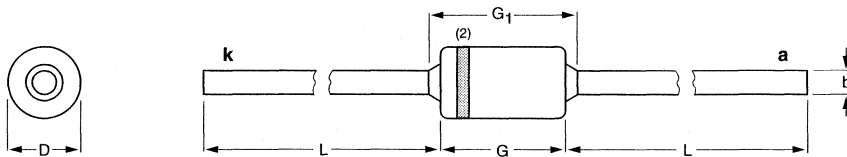
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD80C	100H01				97-06-20

Package outlines

Chapter 2

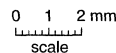
Hermetically sealed glass package;  
Implotec™(1) technology; axial leaded; 2 leads

SOD81



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	G <sub>1</sub> max.	L min.
mm	0.81	2.15	3.8	5	28



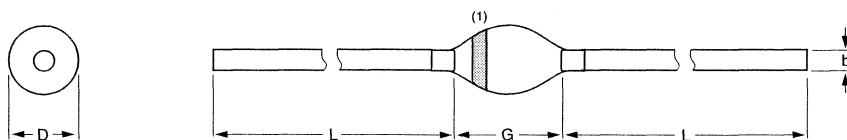
Note

1. Implotec is a trademark of Philips.
2. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD81						97-06-20

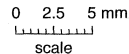
Hermetically sealed glass package; axial leaded; 2 leads

SOD83A



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	1.35	4.5	7.5	30.7



Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD83A						

Package outlines

Chapter 2

Hermetically sealed glass surface mounted package; 2 connectors; Implotec™(1) technology

SOD87

**DIMENSIONS (mm are the original dimensions)**

UNIT	D	D1	H	L
mm	2.1 2.0	2.0 1.8	3.7 3.3	0.3

0 1 2 mm scale

**Note**  
 1. Implotec is a trademark of Philips.  
 2. The marking indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD87	100H03					97-06-20

Hermetically sealed glass package; axial leaded; 2 leads

SOD88A

**DIMENSIONS (mm are the original dimensions)**

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.8	8	30.5

0 2.5 5 mm scale

**Note**  
 1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD88A						97-06-20

Package outlines

Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads

SOD88B

**DIMENSIONS (mm are the original dimensions)**

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.8	11	29

**Note**  
1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD88B						97-06-20

Hermetically sealed glass package; axial leaded; 2 leads

SOD89A

**DIMENSIONS (mm are the original dimensions)**

UNIT	b max.	D max.	G max.	L min.	L <sub>1</sub> max.
mm	1.35	5.5	7	31	3

**Note**  
1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD89A						97-06-20

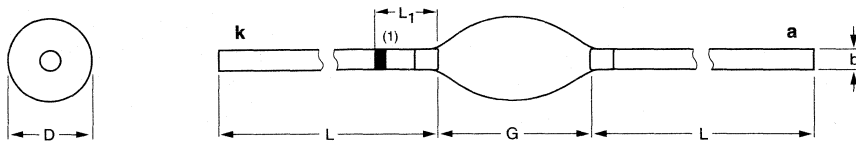


Package outlines

Chapter 2

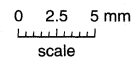
Hermetically sealed glass package; axial leaded; 2 leads

SOD89B



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.	L <sub>1</sub> max.
mm	1.35	5.5	10	29.5	3



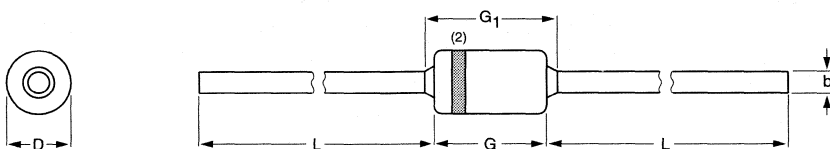
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD89B						97-06-20

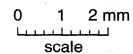
Hermetically sealed glass package; Implotec™(1) technology; axial leaded; 2 leads

SOD91



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	G <sub>1</sub> max.	L min.
mm	0.55	1.7	3.0	3.5	29



Note

1. Implotec is a trademark of Philips.

2. The marking band indicates the cathode.

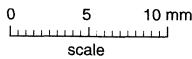
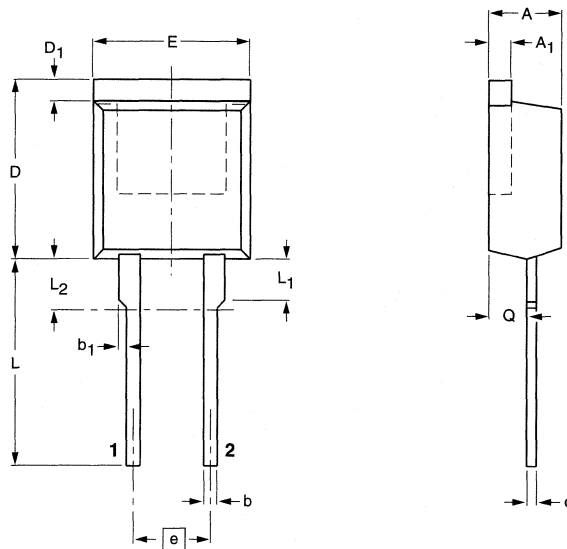
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD91						97-06-09

Package outlines

Chapter 2

Plastic single-ended package; 2-lead low-profile TO-220

SOD95



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max	Q
mm	4.5	1.39	0.9	1.3	0.7	11.0	1.5	10.3	5.08	15.0	3.30	3.0	2.6
	4.1	1.27	0.7	1.0	0.4	10.0	1.1	9.7		13.5	2.79		2.2

Note

1. Terminals in this zone are not tinned.

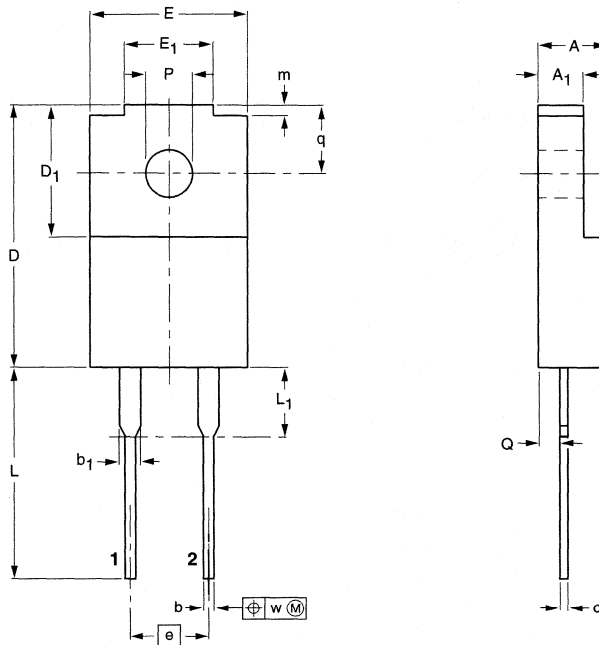
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD95		low-profile 2-lead TO-220				97-06-11

Package outlines

Chapter 2

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 2-lead TO-220F exposed tabs

SOD100



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	L	L <sub>1</sub> <sup>(1)</sup>	m	P	Q	q	w
mm	4.4 4.0	2.9 2.5	0.9 0.7	1.5 1.3	0.55 0.38	17.0 16.4	7.9 7.5	10.2 9.6	5.7 5.3	5.08	14.3 13.5	4.8 4.0	0.9 0.5	3.2 3.0	1.4 1.2	4.4 4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

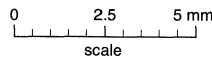
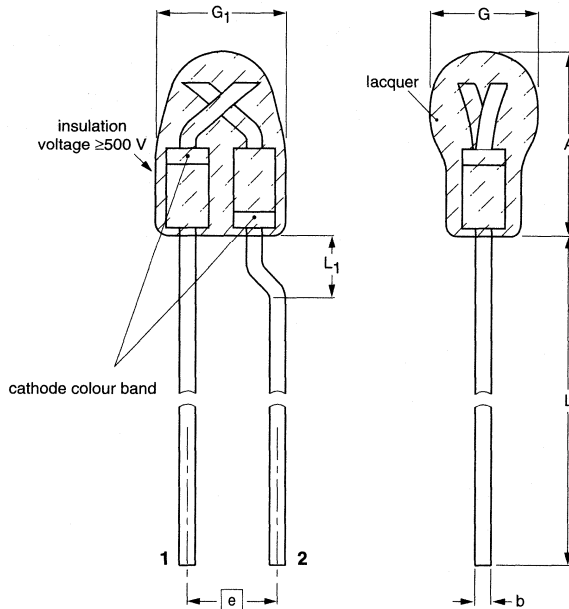
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD100		2-lead TO-220F			97-06-11

Package outlines

Chapter 2

Lacquered glass single-ended package; 2 in-line leads

SOD103



DIMENSIONS (mm are the original dimensions)

UNIT	A	$\varnothing b$	e	G	$G_1$	L max.	$L_1$
mm	7.5 6.0	0.55 0.48	2.54	3.5 2.7	4.2 3.2	14.5	3.5 2.5

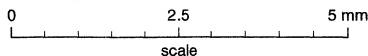
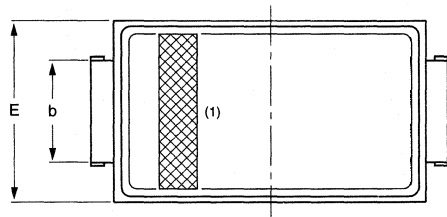
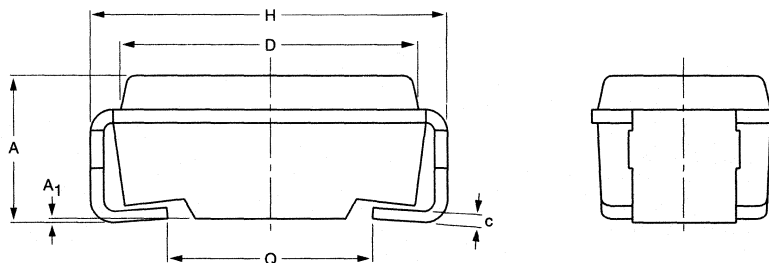
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD103						97-05-21

Package outlines

Chapter 2

Transfer-moulded thermo-setting plastic small rectangular surface mounted package;  
2 connectors

SOD106



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	E	H	Q
mm	2.3 2.0	0.05	1.6 1.4	0.2	4.5 4.3	2.8 2.4	5.5 5.1	3.3 2.7

Note

1. The marking band indicates the cathode.

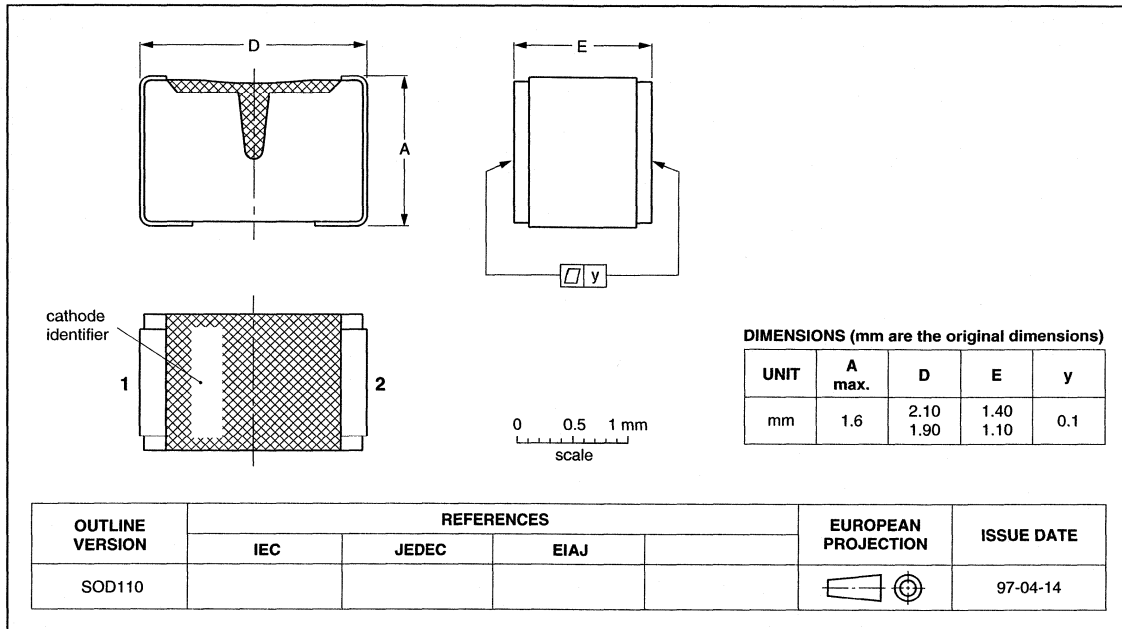
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD106		DO-214AC				97-06-09

Package outlines

Chapter 2

Very small ceramic rectangular surface mounted package

SOD110

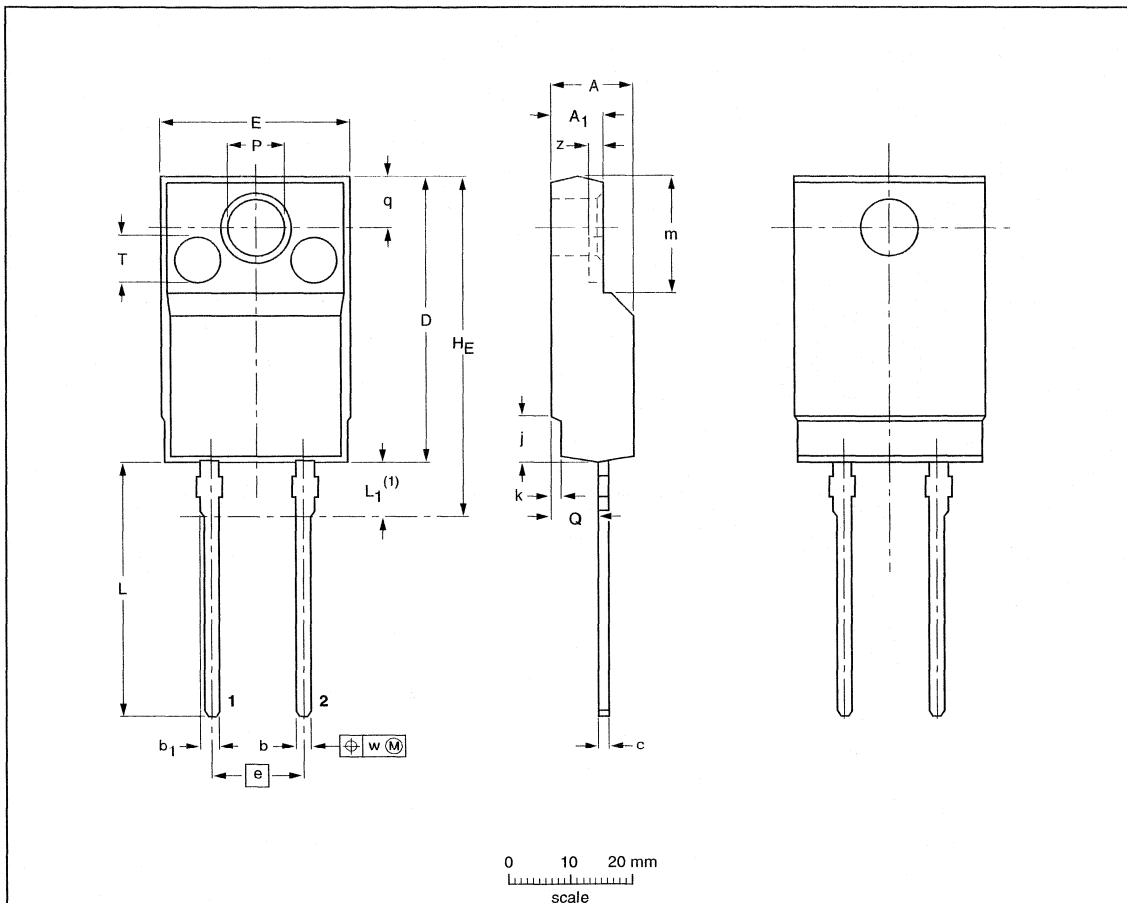


Package outlines

Chapter 2

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 2-leads TO-220 'full pack'

SOD113



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	E	e	H <sub>E</sub> max.	j	k	L	L <sub>1</sub> <sup>(1)</sup>	m	P	Q	q	T	w	z <sup>(2)</sup>
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	0.7 0.4	15.8 15.2	10.3 9.7	5.08	19.0	2.7 2.3	0.6 0.4	14.4 13.5	3.3 2.8	6.5 6.3	3.2 3.0	2.6 2.3	2.6	2.55	0.4	0.8

**Notes**

- 1. Terminals are uncontrolled within zone L<sub>1</sub>.
- 2. z is depth of T.

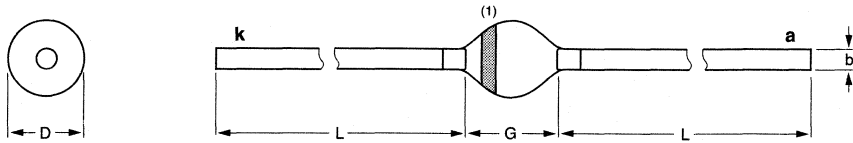
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD113		2-lead TO-220				97-06-11

Package outlines

Chapter 2

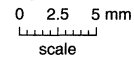
Hermetically sealed glass package; axial leaded; 2 leads

SOD115



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	1.35	5.5	6.0	27



Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD115					97-06-20

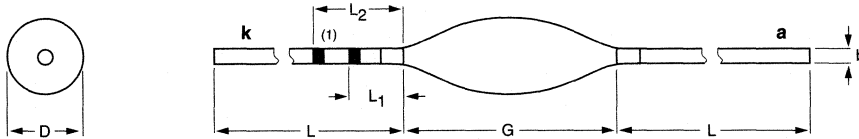


## Package outlines

## Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads

SOD116A to AK



DIMENSIONS (mm are the original dimensions)

OUTLINE VERSION	UNIT	b	D max.	G max.	L min.	L <sub>1</sub> max.	L <sub>2</sub> max.
SOD116A	mm	0.5	2.5	5.5	31.7	3	5
SOD116C	mm	0.5	2.5	7	31	3	5
SOD116E	mm	0.5	2.5	9.5	29.7	3	5
SOD116K	mm	0.5	2.5	12.5	28.2	3	5
SOD116G	mm	0.5	2.5	11	29	3	5
SOD116H	mm	0.5	2.5	3.5	32.7	3	5
SOD116AA	mm	0.5	2.5	3.5	32.8	3	5
SOD116AB	mm	0.5	2.5	5.5	31.8	3	5
SOD116AC	mm	0.5	2.5	8.3	30.4	3	5
SOD116AD	mm	0.5	2.5	8.7	30.2	3	5
SOD116AE	mm	0.5	2.5	9.1	30	3	5
SOD116AF	mm	0.5	2.5	9.5	29.8	3	5
SOD116AG	mm	0.5	2.5	9.9	29.6	3	5
SOD116AH	mm	0.5	2.5	10.5	29.3	3	5
SOD116AI	mm	0.5	2.5	11.5	28.8	3	5
SOD116AJ	mm	0.5	2.5	12.5	28.3	3	5
SOD116AK	mm	0.5	2.5	13.5	27.8	3	5

## Note

1. The marking bands indicate the cathode.

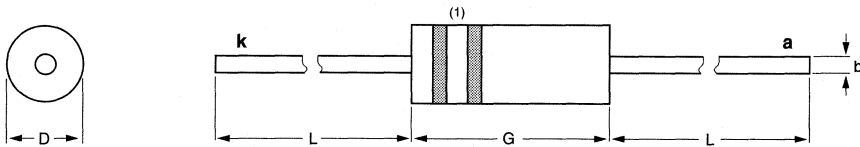
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD116A to AK						97-06-18

Package outlines

Chapter 2

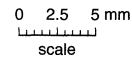
Hermetically sealed glass package; axial leaded; 2 leads

SOD118A



DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.52 0.48	2.6 2.4	6.7 6.3	31



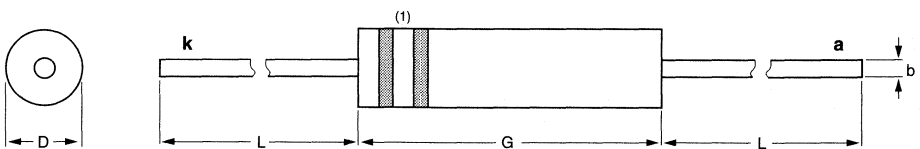
Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD118A					97-06-20

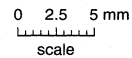
Hermetically sealed glass package; axial leaded; 2 leads

SOD118B



DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.52 0.48	2.6 2.4	10.2 9.8	29



Note

1. The marking bands indicate the cathode.

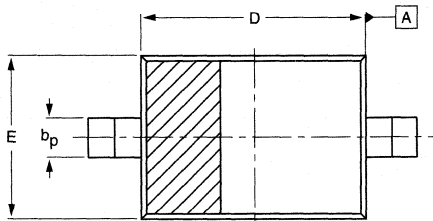
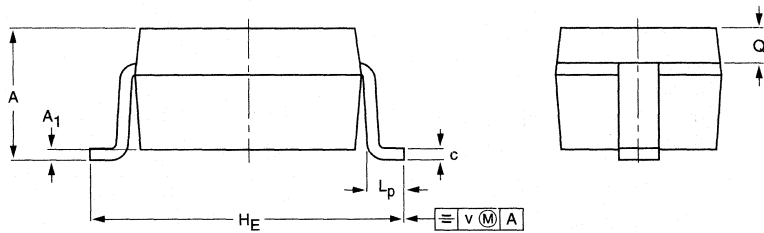
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOD118B					97-06-20

Package outlines

Chapter 2

Plastic surface mounted package; 2 leads

SOD323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	H <sub>E</sub>	L <sub>p</sub>	Q	v
mm	1.1 0.8	+0.05 -0.05	0.40 0.25	0.25 0.10	1.8 1.6	1.35 1.15	2.7 2.3	0.45 0.15	0.25 0.15	0.2

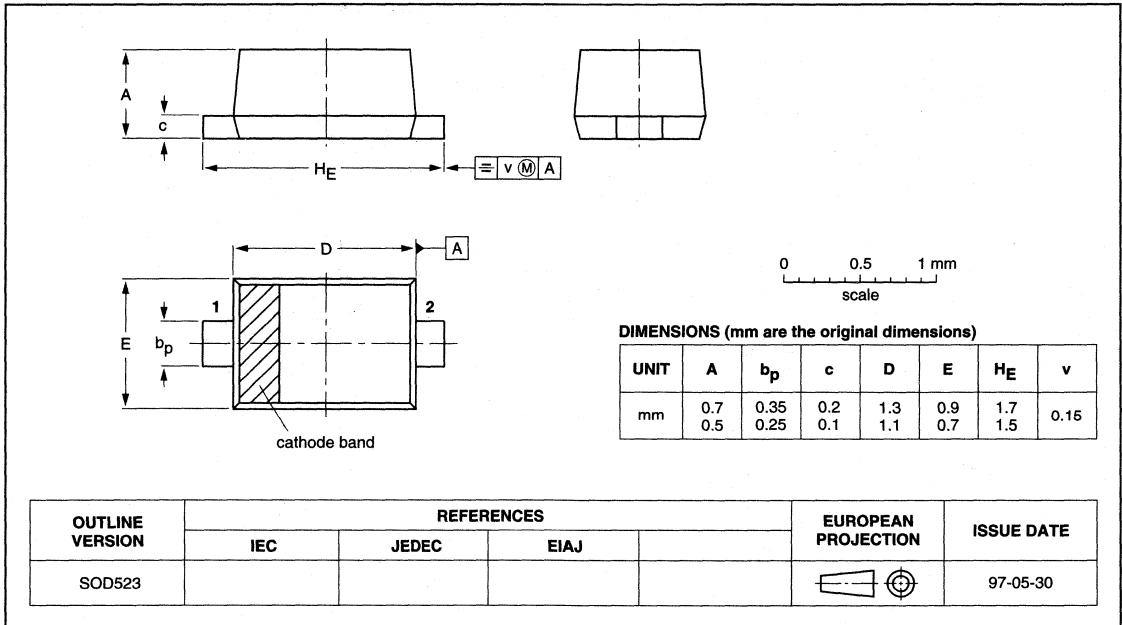
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD323						97-06-02

Package outlines

Chapter 2

Plastic surface mounted package; 2 leads

SOD523

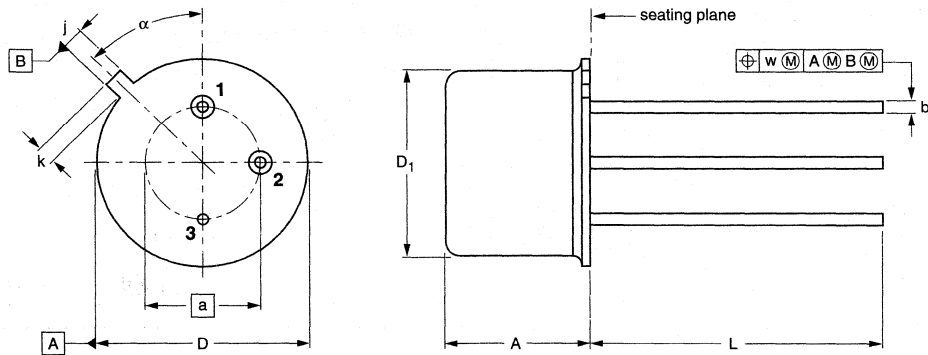


Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 3 leads

SOT5/11



DIMENSIONS (mm are the original dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	6.60 6.35	5.08	0.48 0.41	9.39 9.08	8.33 8.18	0.85 0.75	0.95 0.75	14.2 12.7	0.2	45°

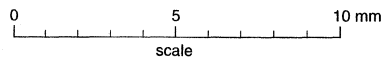
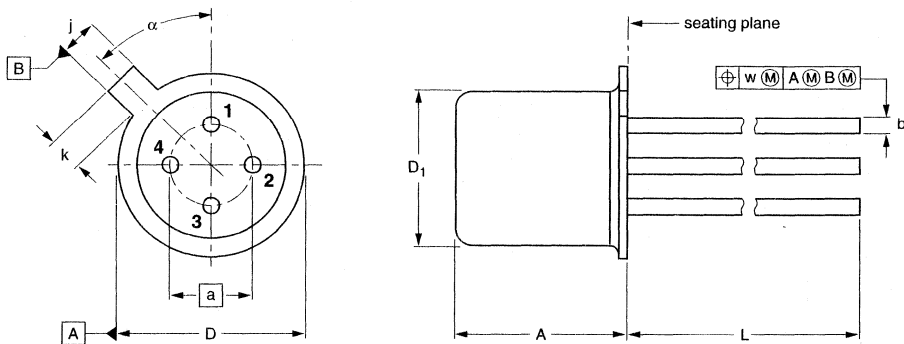
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT5/11		TO-39				97-04-11

Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 4 leads

SOT18/9



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	$\alpha$
mm	5.31 4.74	2.54	0.46 0.42	5.45 5.30	4.70 4.55	1.05 0.95	1.0 0.9	14.5 13.5	0.36	45°

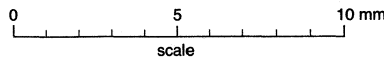
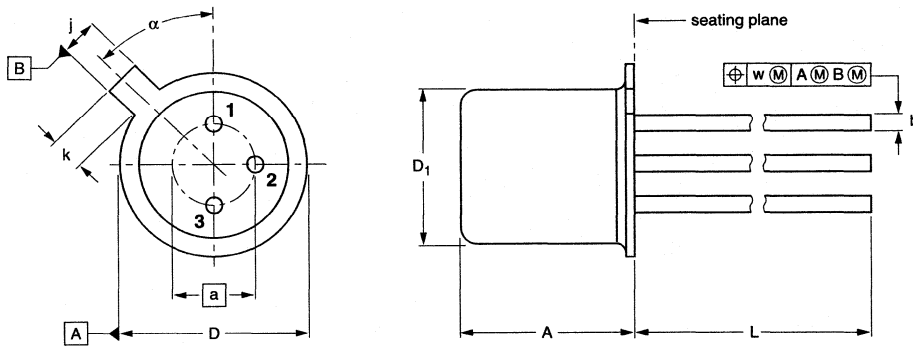
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT18/9	B12/C7 type 3	TO-72				97-04-18

Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 3 leads

SOT18/13



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	5.31 4.74	2.54	0.47 0.41	5.45 5.30	4.70 4.55	1.03 0.94	1.1 0.9	15.0 12.7	0.40	45°

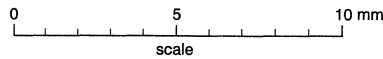
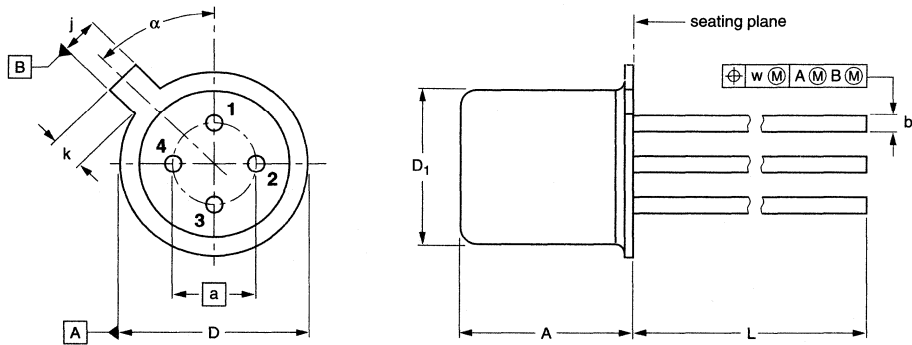
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT18/13	B11/C7 type 3	TO-18				97-04-18

Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 4 leads

SOT18/14



**DIMENSIONS** (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	5.31 4.74	2.54	0.46 0.42	5.45 5.30	4.70 4.55	1.03 0.97	1.1 0.9	15.0 13.0	0.40	45°

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT18/14	B12/C7 type 3	TO-72			97-04-18

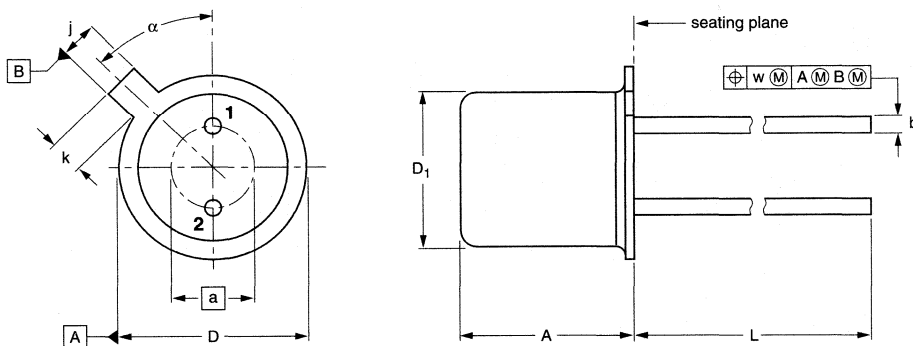


Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 2 leads

SOT18/15



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	5.31 4.74	2.54	0.46 0.42	5.45 5.30	4.70 4.55	1.03 0.97	1.1 0.9	15.0 13.0	0.40	45°

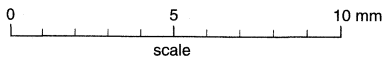
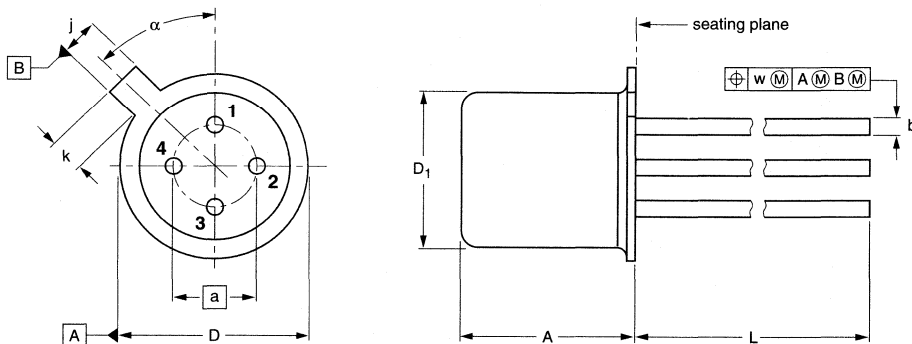
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT18/15	B10/C7	TO-18			97-04-18

Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 4 leads

SOT18/17



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	5.31 4.74	2.54	0.46 0.42	5.45 5.30	4.70 4.55	1.03 0.97	1.1 0.9	15.0 13.0	0.40	45°

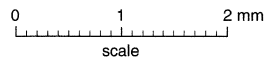
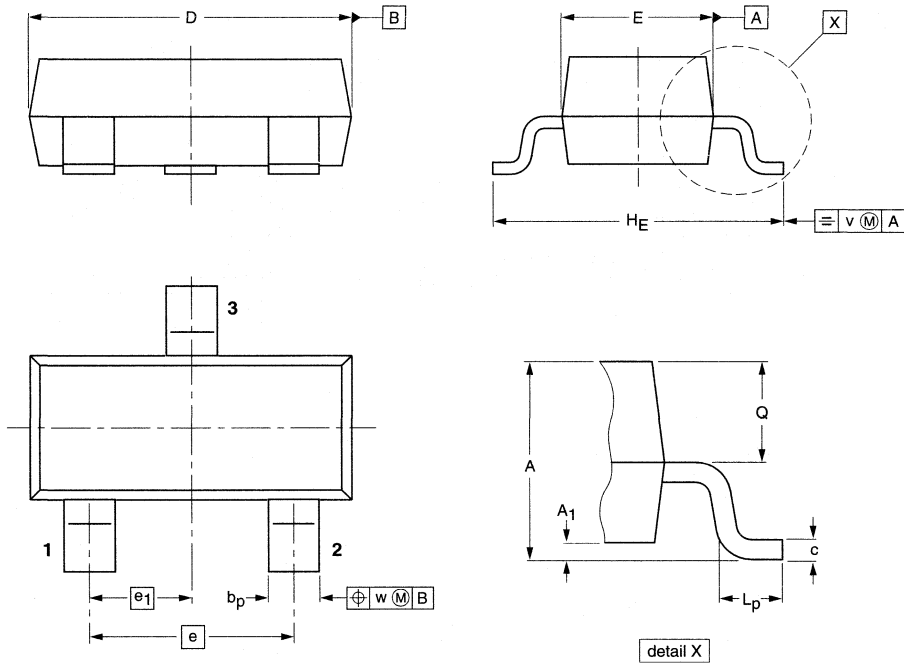
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT18/17	B12/C7 type 3	TO-72				97-04-18

Package outlines

Chapter 2

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

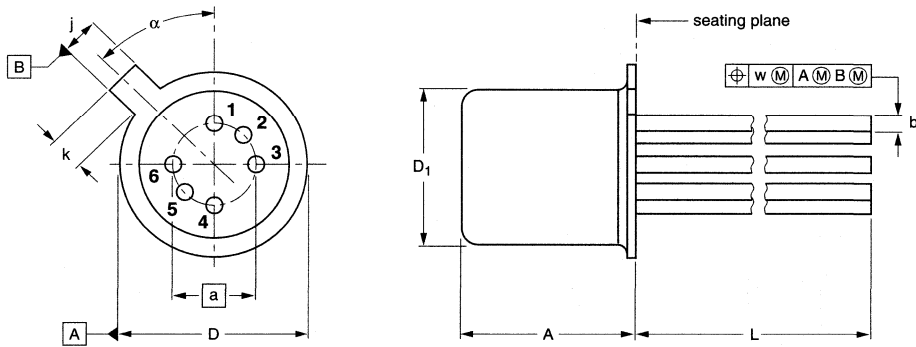
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT23					97-02-28

Package outlines

Chapter 2

Metal-can cylindrical single-ended package; 6 leads

SOT31



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

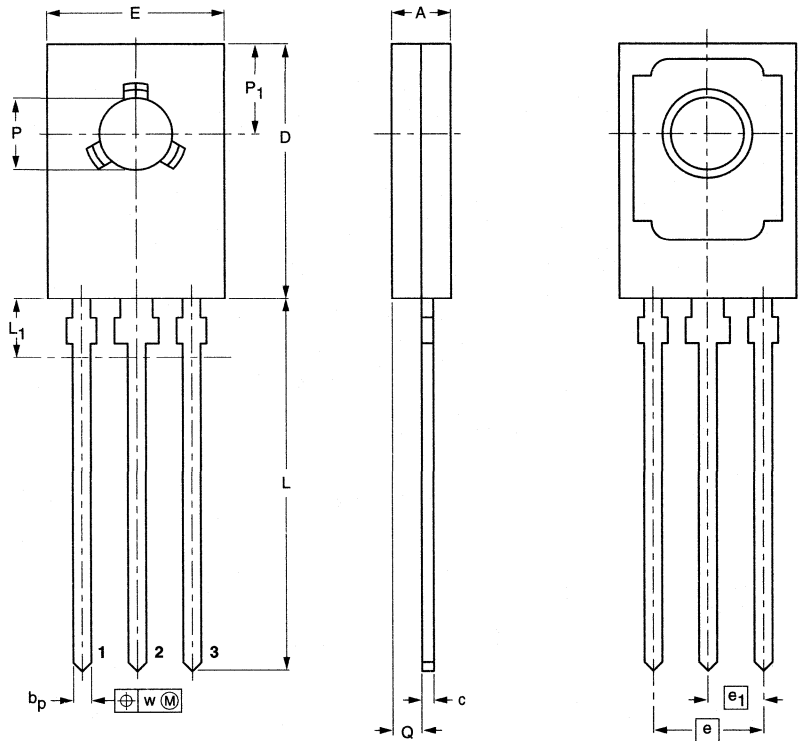
UNIT	A max.	a	b max.	D max.	D <sub>1</sub> max.	j max.	k max.	L min.	w	α
mm	5.3	2.54	0.51	5.8	4.8	1.16	1.17	12.7	0.35	45°

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT31		TO-71			97-06-18

Package outlines

Chapter 2

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max	Q	P	P <sub>1</sub>	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

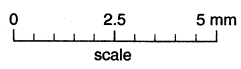
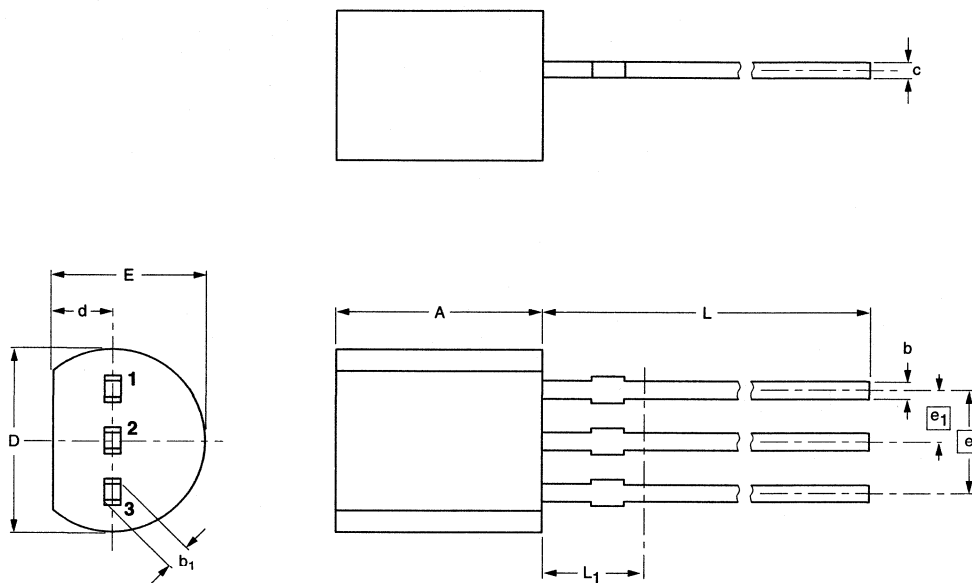
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT32		TO-126			97-03-04

Package outlines

Chapter 2

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

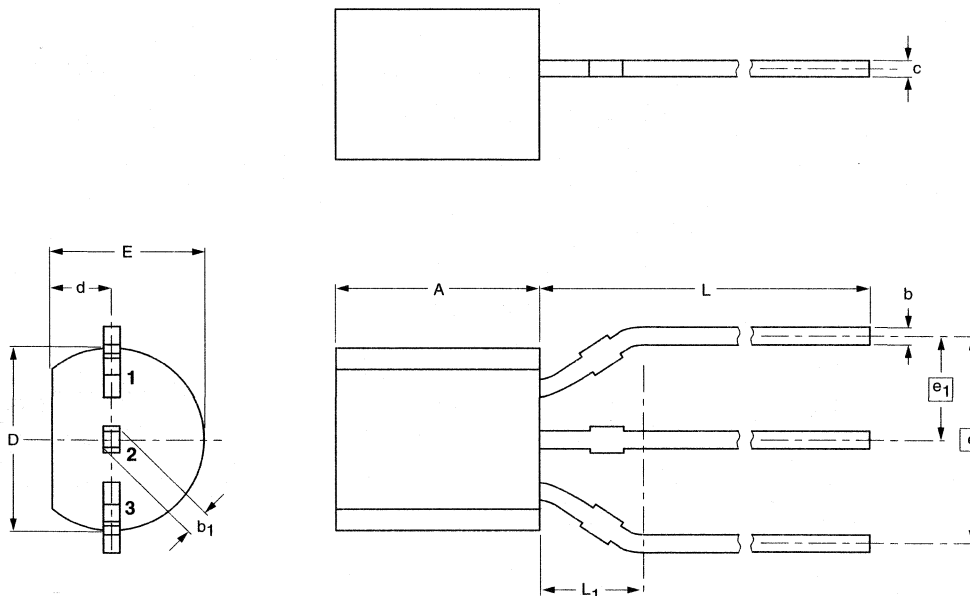
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Package outlines

Chapter 2

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)

SOT54A



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	5.08	2.54	14.5 12.7	2.5

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

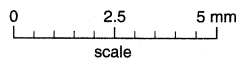
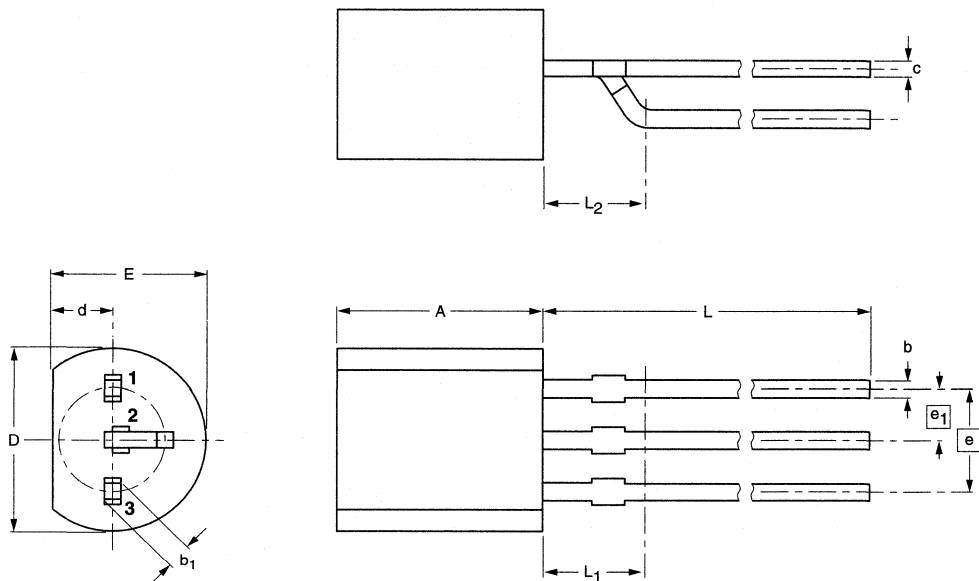
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54A		TO-92	SC-43			97-05-13

Package outlines

Chapter 2

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	d	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max	L <sub>2</sub> max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14

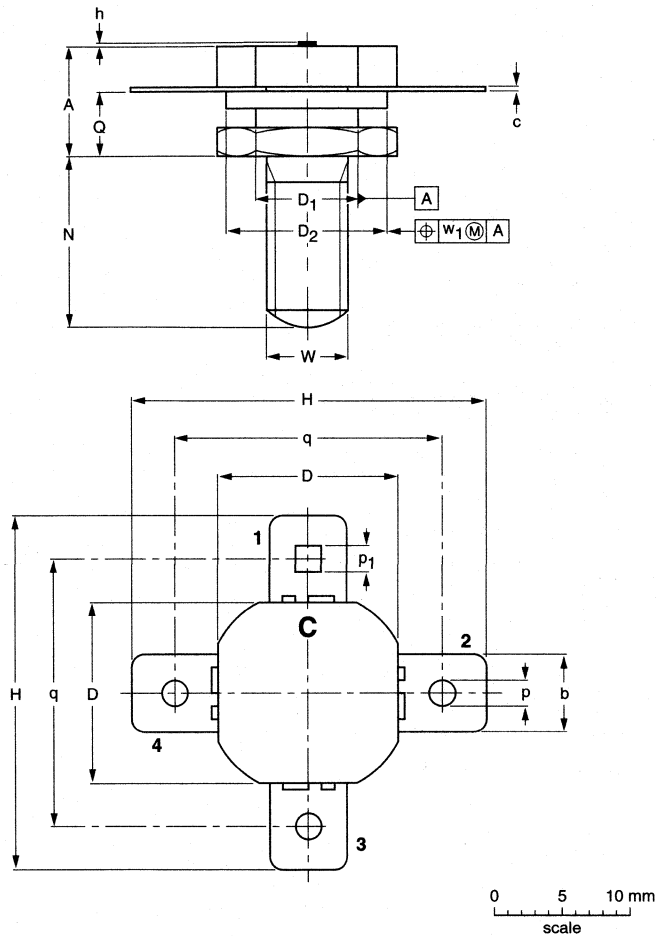


Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT55E



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	H	h	N	p	p <sub>1</sub>	Q	q	W	w <sub>1</sub>
mm	8.51 7.18	6.13 5.86	0.31 0.20	14.10 13.84	8.13 7.87	12.83 12.57	27.44 26.41	0.26 0.05	13.39 12.62	1.94 1.67	1.94 1.67	5.03 4.52	21.14 20.87	1/4"× 28 UNF	0.51
inches	0.335 0.283	0.241 0.231	0.012 0.008	0.555 0.545	0.320 0.310	0.505 0.495	1.080 1.040	0.010 0.002	0.527 0.497	0.076 0.066	0.076 0.066	0.198 0.178	0.832 0.822		0.02

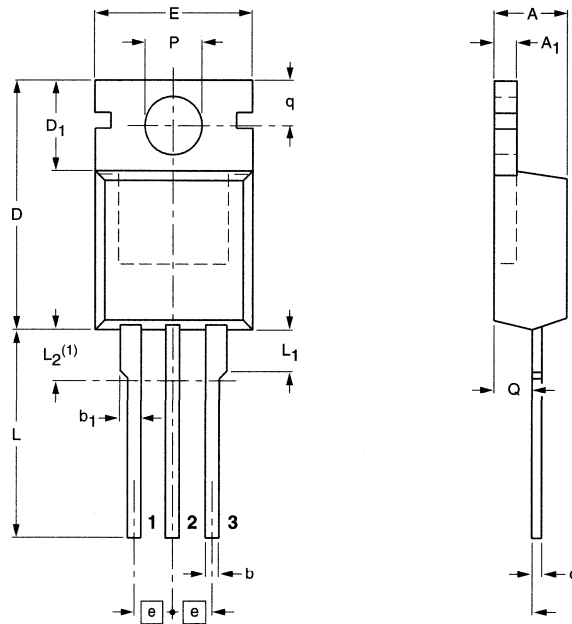
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT55E						97-06-28

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

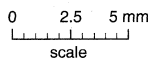
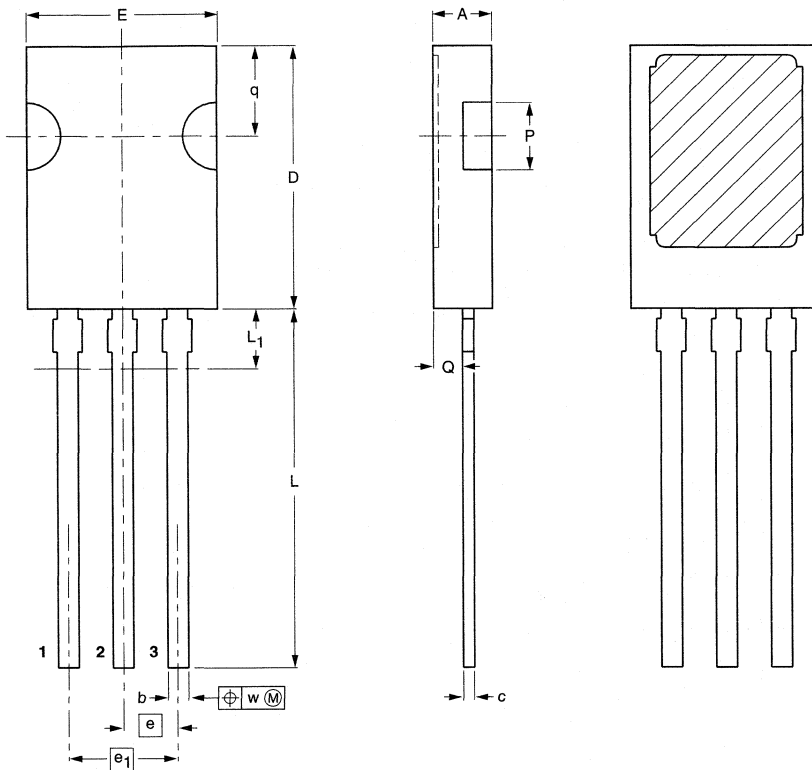
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11

Package outlines

Chapter 2

Plastic single-ended package; 3 leads (in-line)

SOT82



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.	P	Q	q	w
mm	2.8 2.3	0.88 0.65	0.58 0.47	11.1 10.5	7.8 7.2	2.29	4.58	16.5 15.3	2.54	3.1 2.5	1.5 0.9	3.9 3.5	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

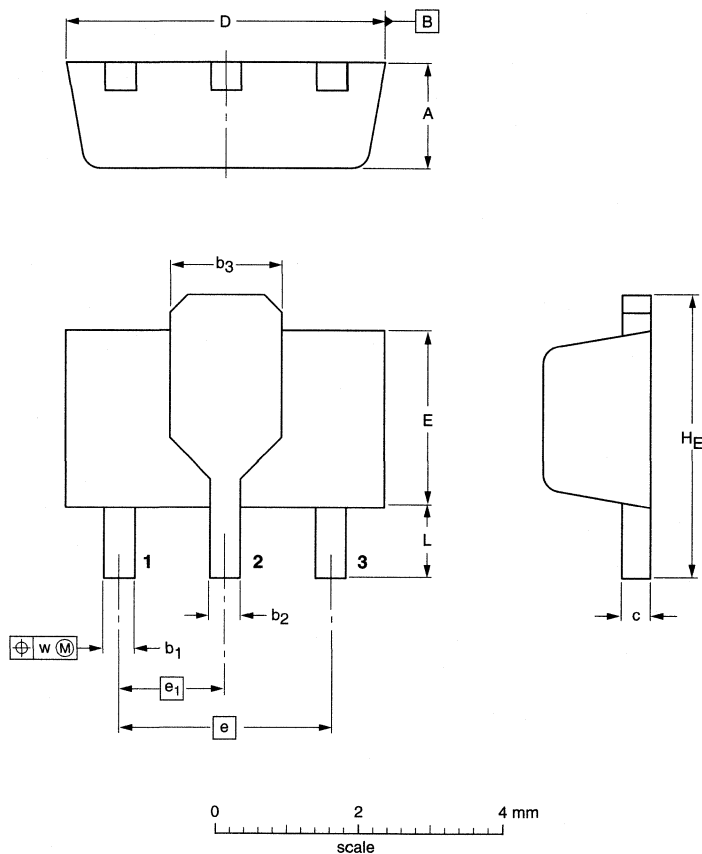
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT82					97-06-11

Package outlines

Chapter 2

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

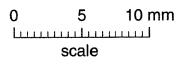
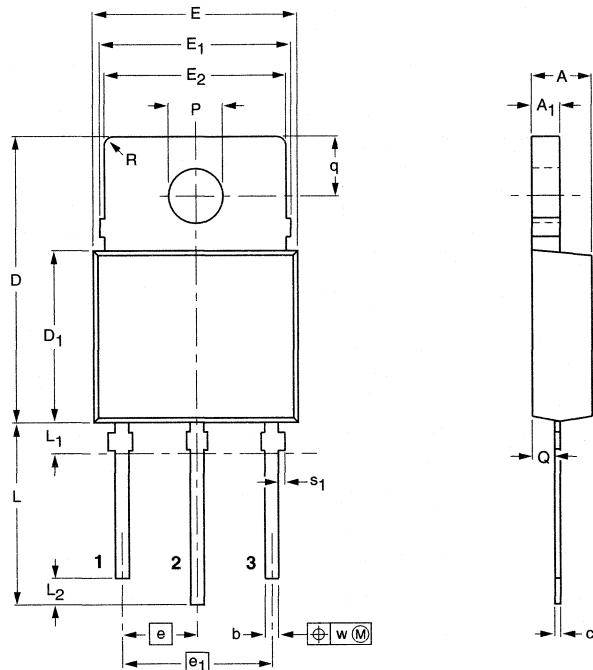
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT89					97-02-28

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)

SOT93A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	E <sub>2</sub>	e	e <sub>1</sub>	L <sup>(1)</sup>	L <sub>1</sub> <sup>(2)</sup> max.	L <sub>2</sub>	P	Q	q	R	s <sub>1</sub>	w
mm	4.6 4.4	2.05 1.95	1.15 0.95	0.50 0.35	21 20	12.7 12.3	15.2 14.8	14.15 13.85	13.8 13.4	5.5	11.0	14.1 13.6	2.2	2	4.25 4.15	1.7 1.5	4.55 4.25	2 1	0.7 0.5	0.5

Notes

- Dimensions are for untinned terminals.
- Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

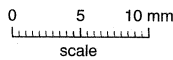
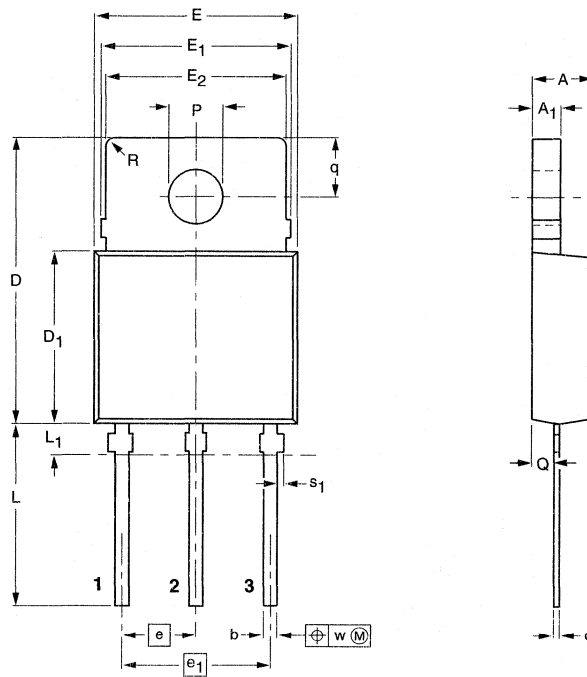
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT93A						97-06-11

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)

SOT93B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	E <sub>2</sub>	e	e <sub>1</sub>	L <sup>(1)</sup>	L <sub>1</sub> <sup>(2)</sup> max.	P	Q	q	R	s <sub>1</sub>	w
mm	4.6 4.4	2.05 1.95	1.15 0.95	0.50 0.35	21 20	12.7 12.3	15.2 14.8	14.15 13.85	13.8 13.4	5.5	11.0	14.1 13.6	2.2 max	4.25 4.15	1.7 1.5	4.55 4.25	2 1	0.7 0.5	0.5

Notes

- Dimensions are for untinned terminals.
- Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

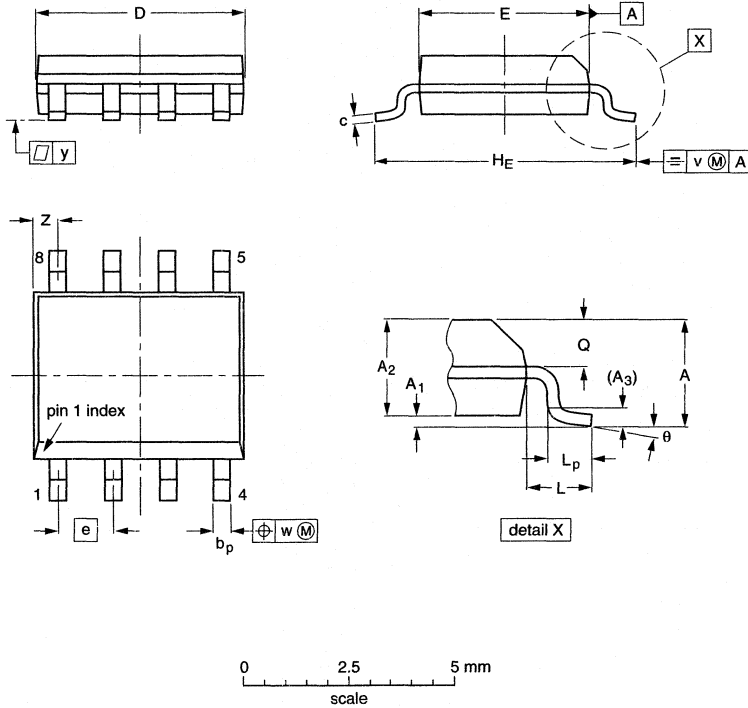
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT93B						97-06-11

Package outlines

Chapter 2

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

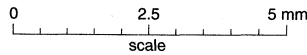
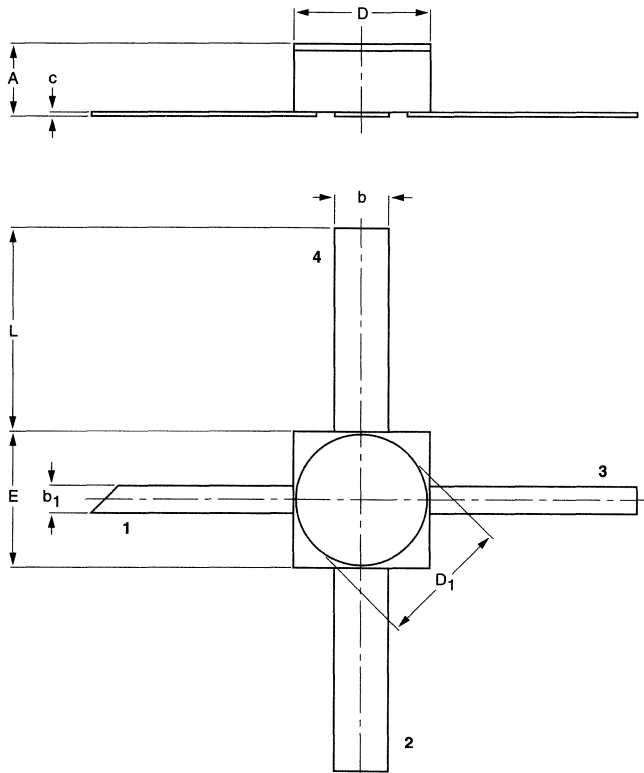
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

Package outlines

Chapter 2

Hermetic ceramic package; 4 leads

SOT100A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	L
mm	1.31 0.81	1.07 0.96	0.56 0.45	0.16 0.07	2.64 2.34	2.6 2.4	2.64 2.34	4.3 3.3

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT100A						97-05-23

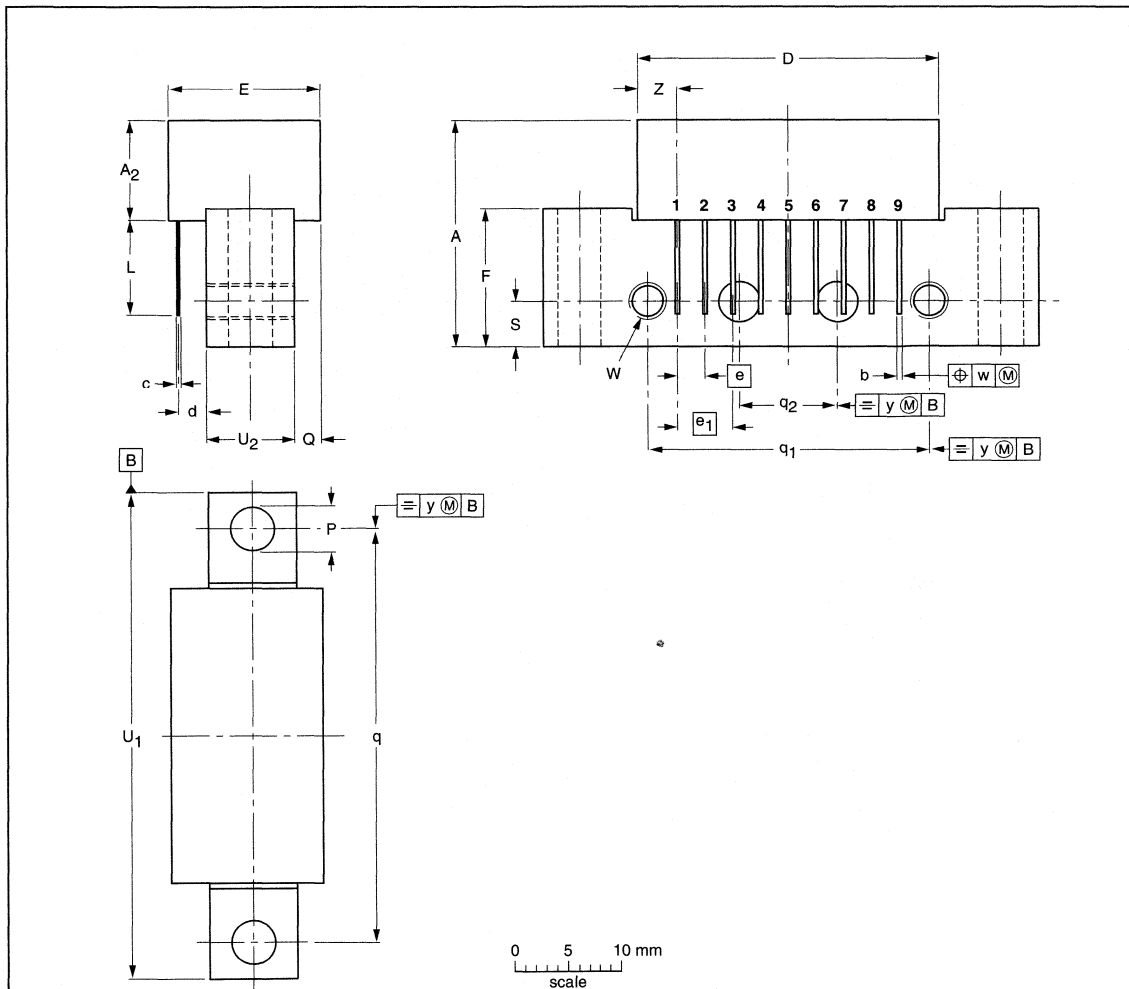


Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 9 gold-plated in-line leads

SOT115D



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	∅ P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>	S	U <sub>1</sub> max.	U <sub>2</sub>	W	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

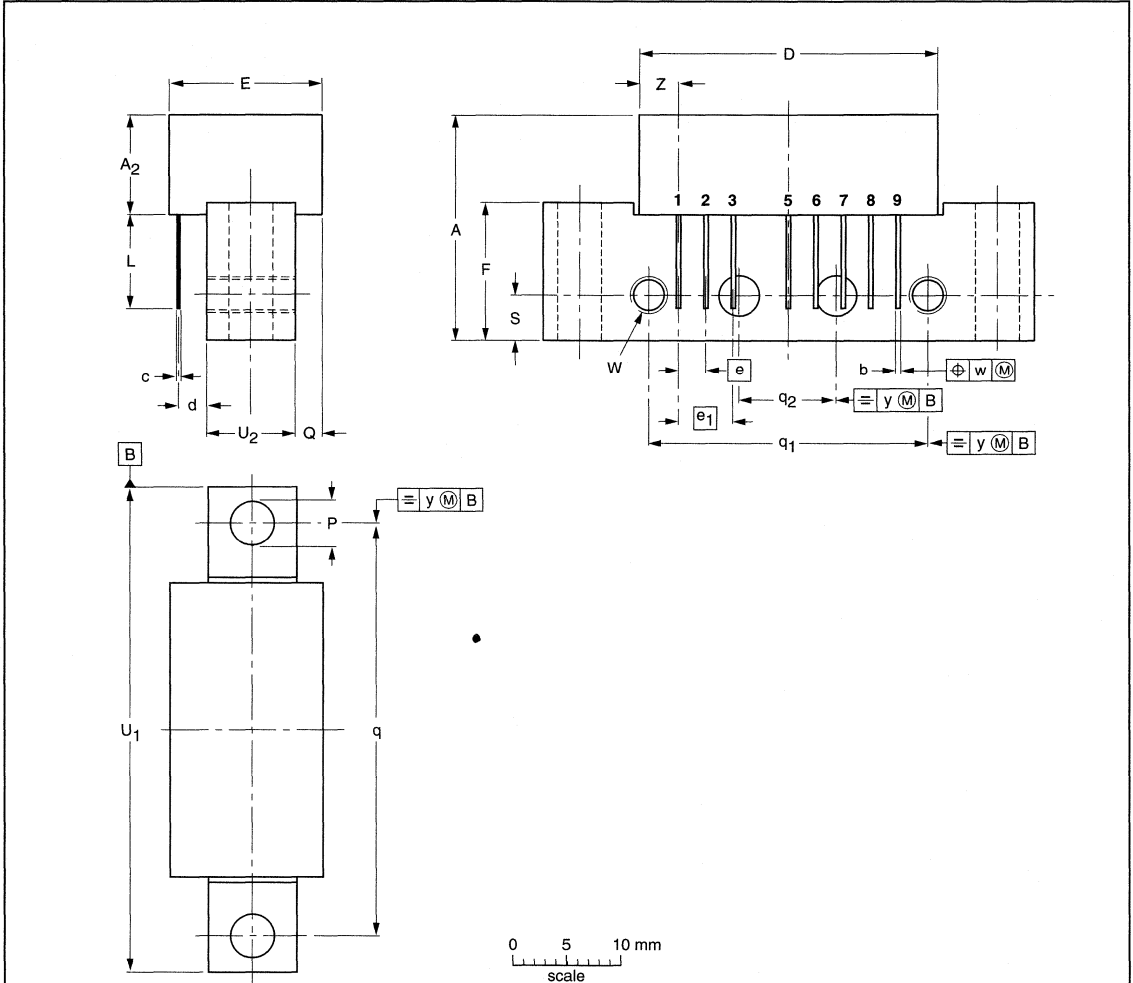
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT115D					97-04-10

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads

SOT115G



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	Ø P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>	s	U <sub>1</sub> max.	U <sub>2</sub>	w	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

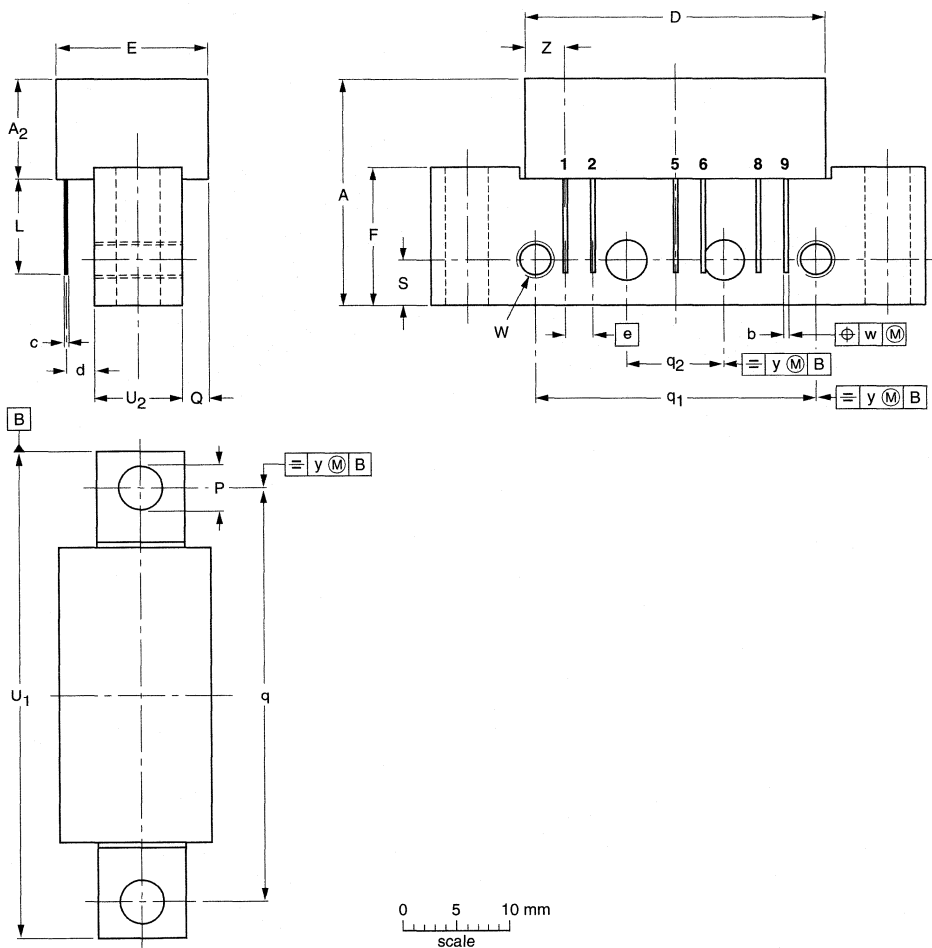
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115G						97-04-10

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 6 gold-plated in-line leads

SOT115H



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	F	L min.	∅ P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>	S	U <sub>1</sub> max.	U <sub>2</sub>	W	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

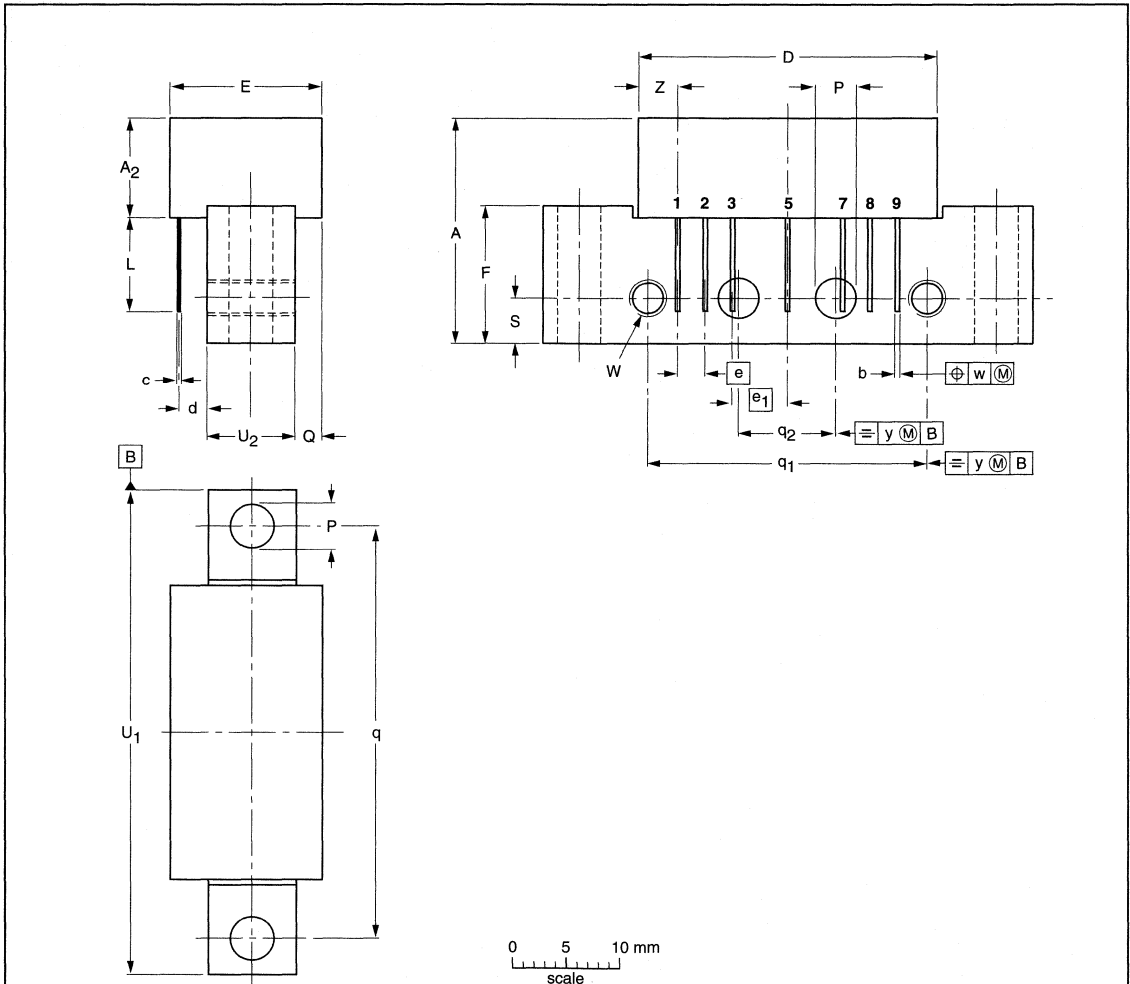
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115H						97-04-10

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 7 gold-plated in-line leads

SOT115J



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	∅ P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>	s	U <sub>1</sub> max.	U <sub>2</sub>	w	y	Z max.	
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

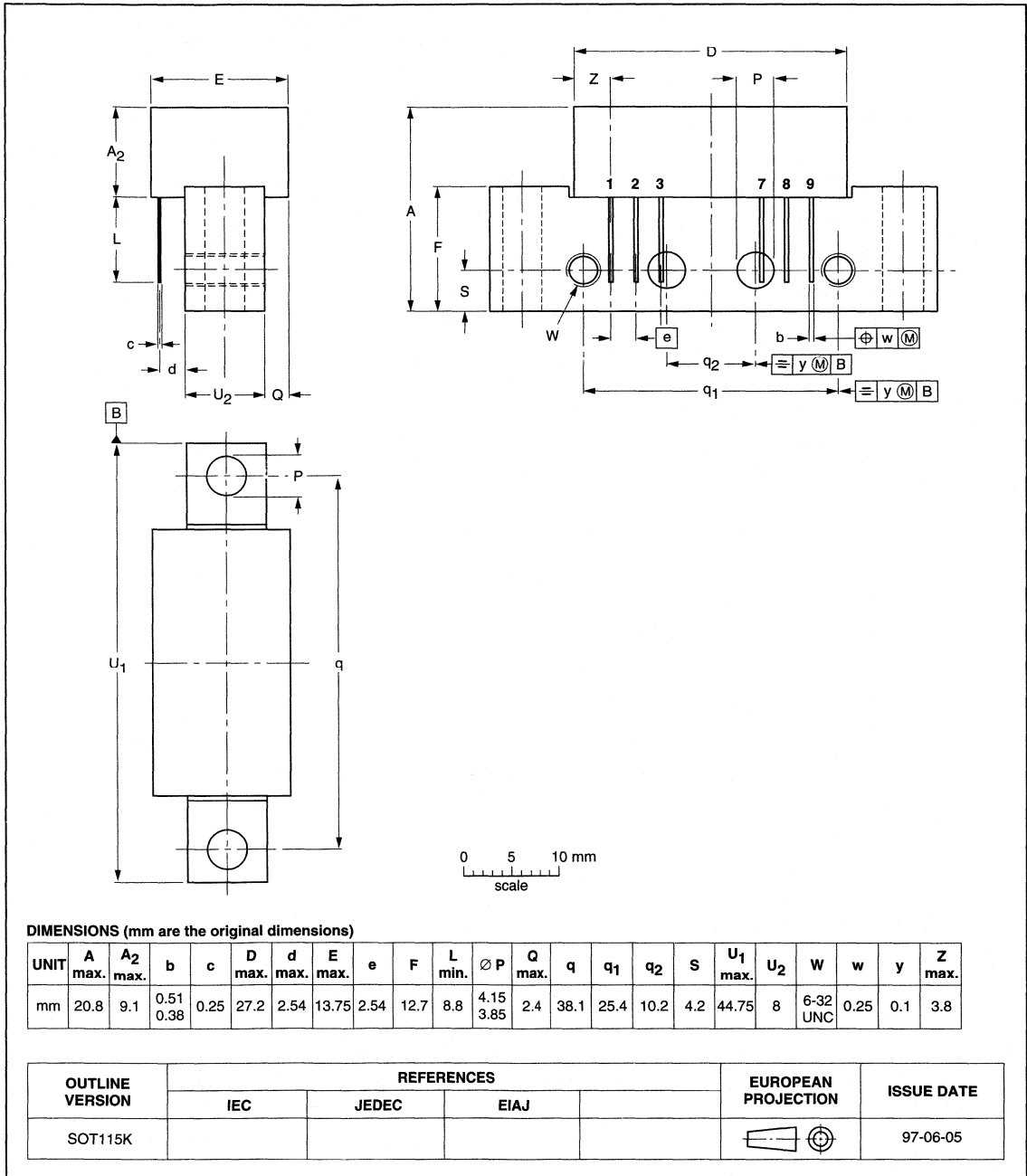
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT115J					97-04-10

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 6 gold-plated in-line leads

SOT115K

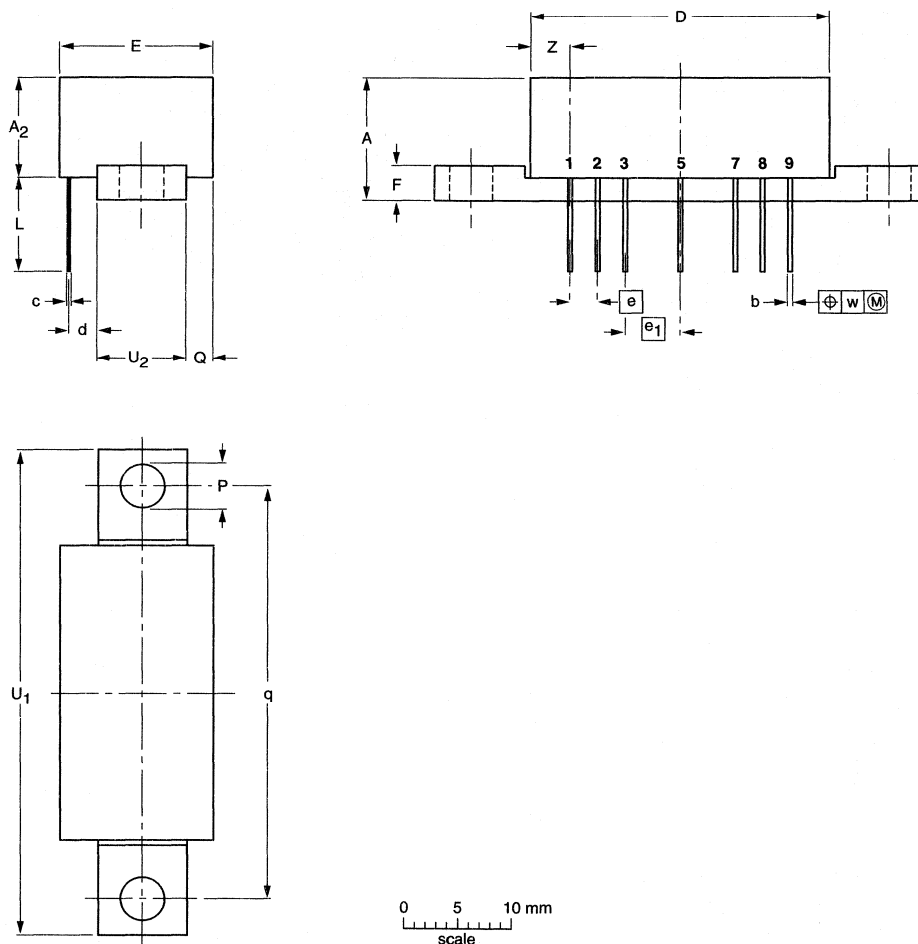


Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange;  
2 vertical mounting holes; 7 gold-plated in-line leads

SOT115L



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	∅ P	Q max.	q	U <sub>1</sub> max.	U <sub>2</sub>	w	Z max.
mm	11.5	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	3.2	8.8	4.15 3.85	2.4	38.1	44.75	8	0.25	3.8

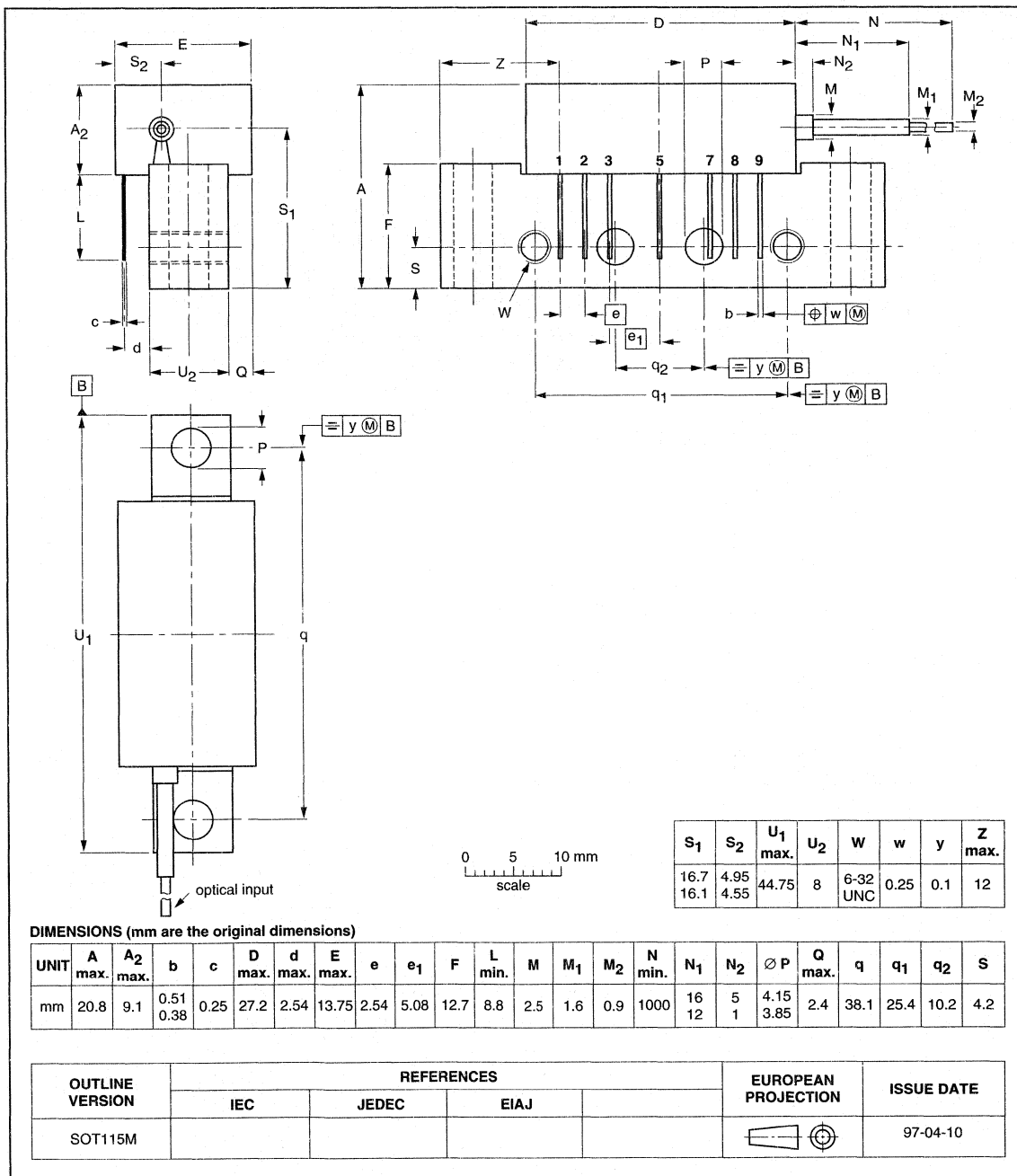
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT115L					97-06-05

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 7 gold-plated in-line leads

SOT115M

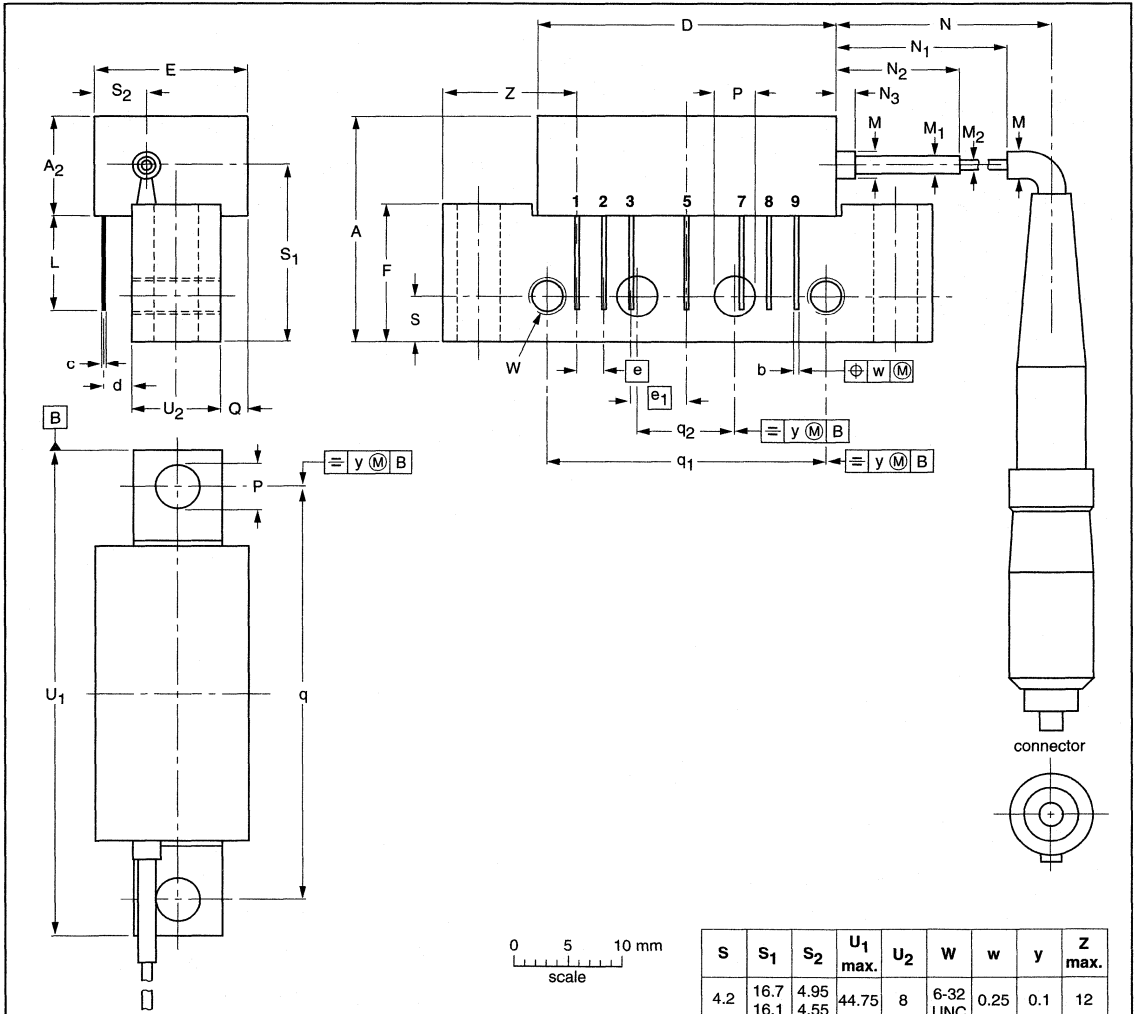


Package outlines

Chapter 2

**Rectangular single-ended flat package; aluminium flange;  
2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes;  
optical input with connector; 7 gold-plated in-line leads**

**SOT115N**



S	S <sub>1</sub>	S <sub>2</sub>	U <sub>1</sub> max.	U <sub>2</sub>	W	w	y	Z max.
4.2	16.7	4.95	44.75	8	6-32 UNC	0.25	0.1	12
	16.1	4.55						

**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	M	M <sub>1</sub>	M <sub>2</sub>	N	N <sub>1</sub>	N <sub>2</sub>	N <sub>3</sub>	∅ P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	627 577	127 77	16 12	5 1	4.15 3.85	2.4	38.1	25.4	10.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115N						97-04-10

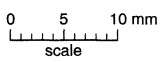
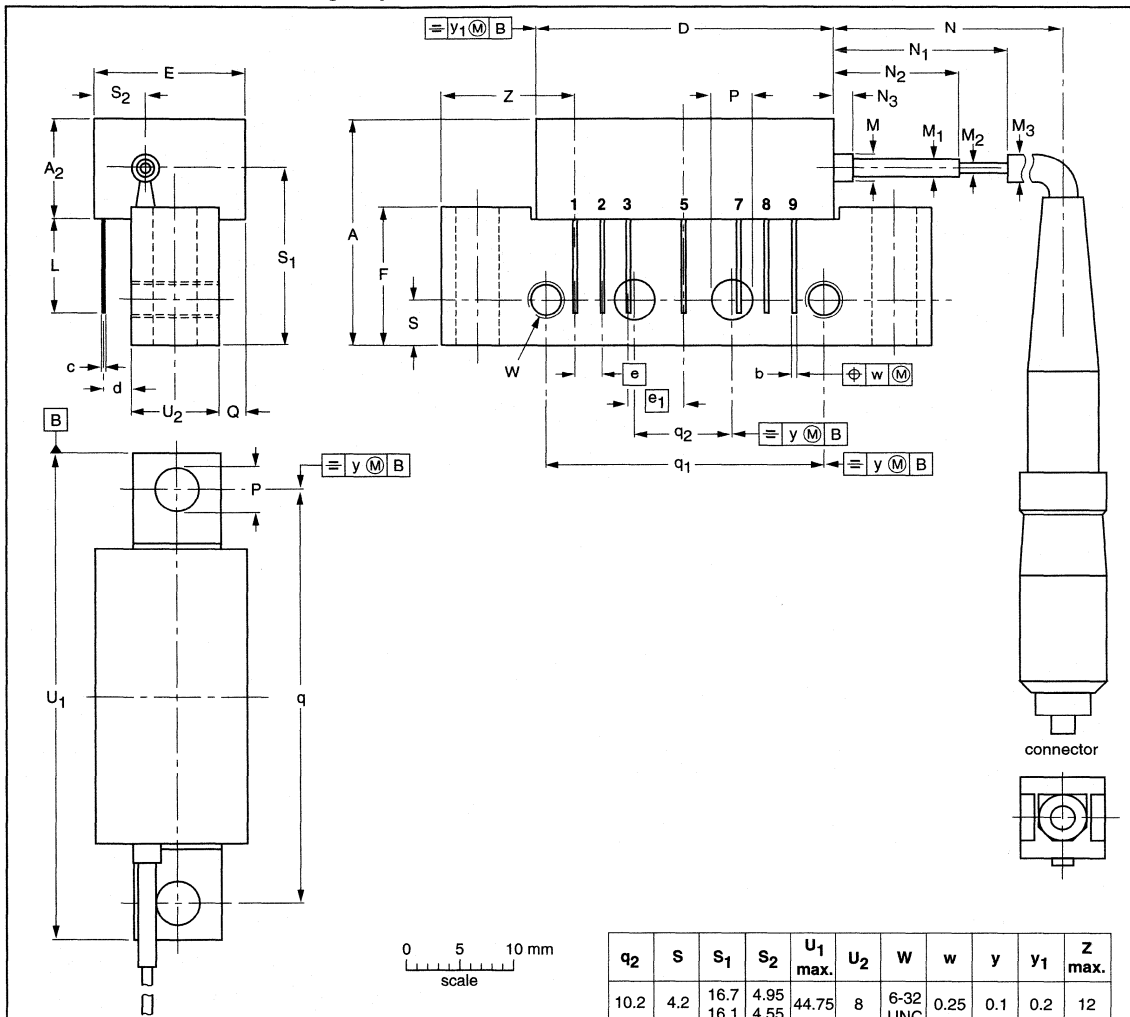


Package outlines

Chapter 2

**Rectangular single-ended flat package; aluminium flange;  
2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes;  
optical input with connector; 7 gold-plated in-line leads**

**SOT115P**



q <sub>2</sub>	S	S <sub>1</sub>	S <sub>2</sub>	U <sub>1</sub> max.	U <sub>2</sub>	W	w	y	y <sub>1</sub>	Z max.
10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	0.2	12

**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	M	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	N	N <sub>1</sub>	N <sub>2</sub>	N <sub>3</sub>	∅ P	Q max.	q	q <sub>1</sub>
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	917 817	18.5 16.0	16	5 1	4.15 3.85	2.4	38.1	25.4

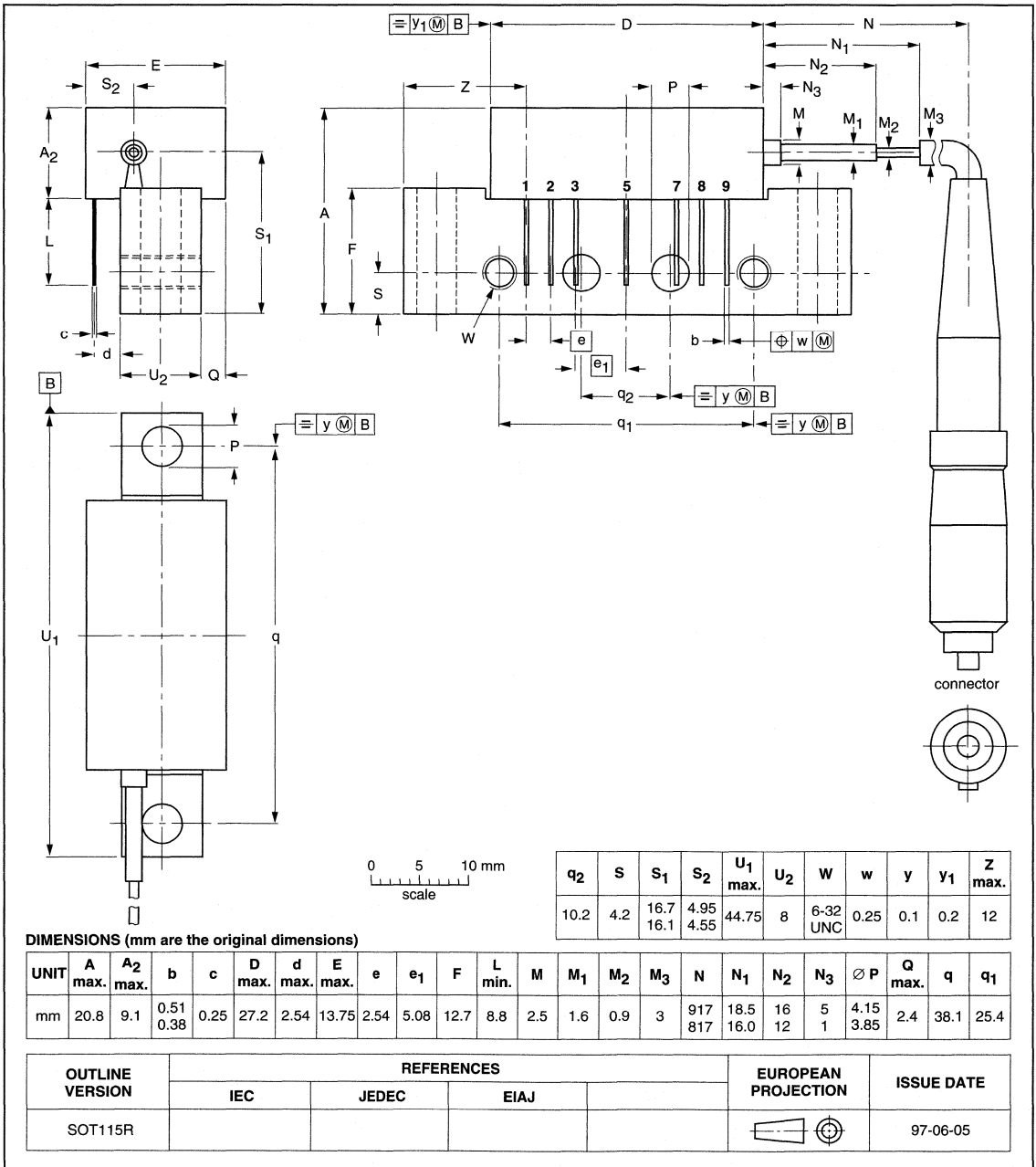
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT115P					97-04-18

Package outlines

Chapter 2

**Rectangular single-ended package; aluminium flange;  
2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes;  
optical input with connector; 7 gold-plated in-line leads**

**SOT115R**

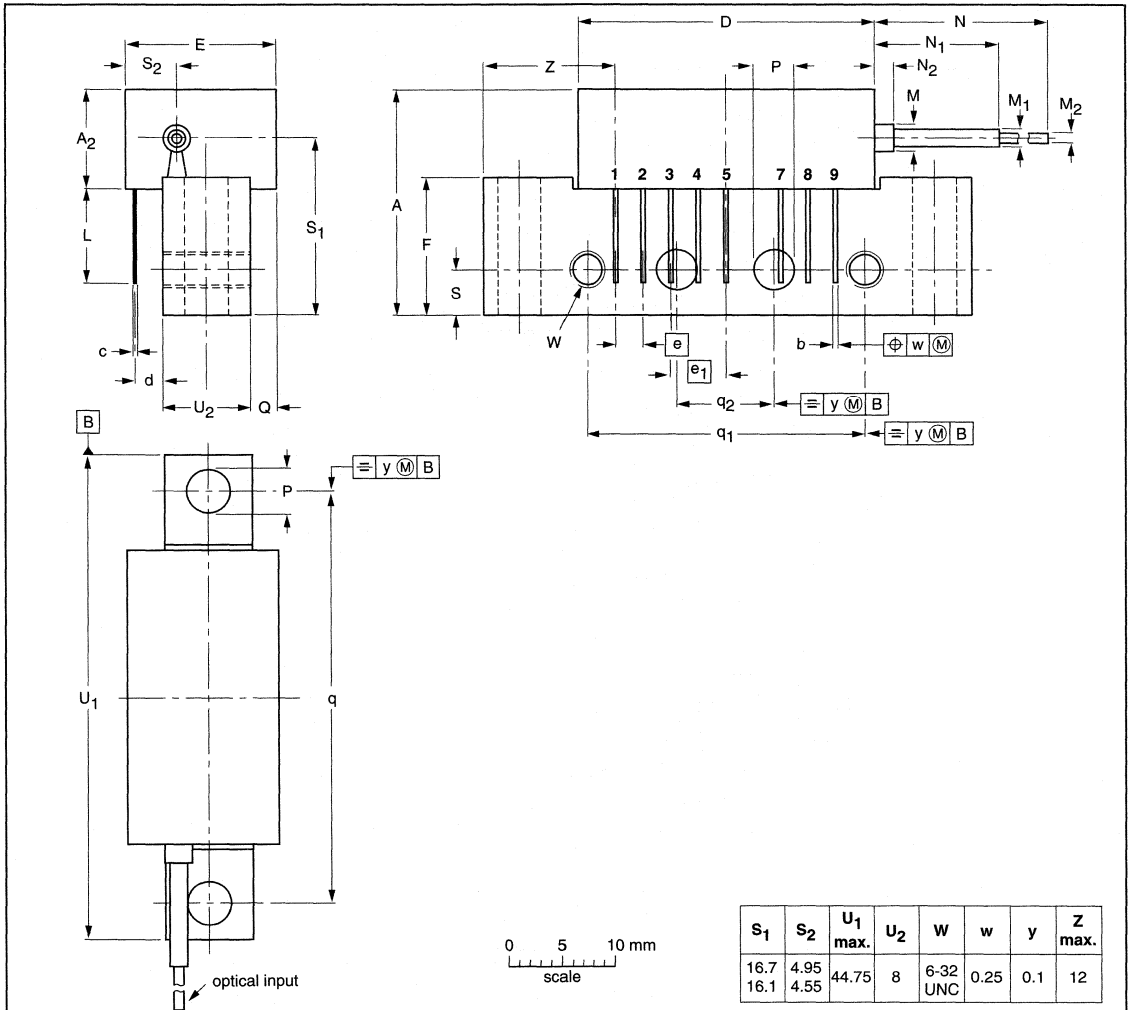


Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 8 gold-plated in-line leads

SOT115T



S <sub>1</sub>	S <sub>2</sub>	U <sub>1</sub> max.	U <sub>2</sub>	W	w	y	Z max.
16.7	4.95	44.75	8	6-32 UNC	0.25	0.1	12
16.1	4.55						

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>2</sub> max.	b	c	D max.	d max.	E max.	e	e <sub>1</sub>	F	L min.	M	M <sub>1</sub>	M <sub>2</sub>	N min.	N <sub>1</sub>	N <sub>2</sub>	∅ P	Q max.	q	q <sub>1</sub>	q <sub>2</sub>	S
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	1000	16 12	5 1	4.15 3.85	2.4	38.1	25.4	10.2	4.2

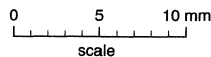
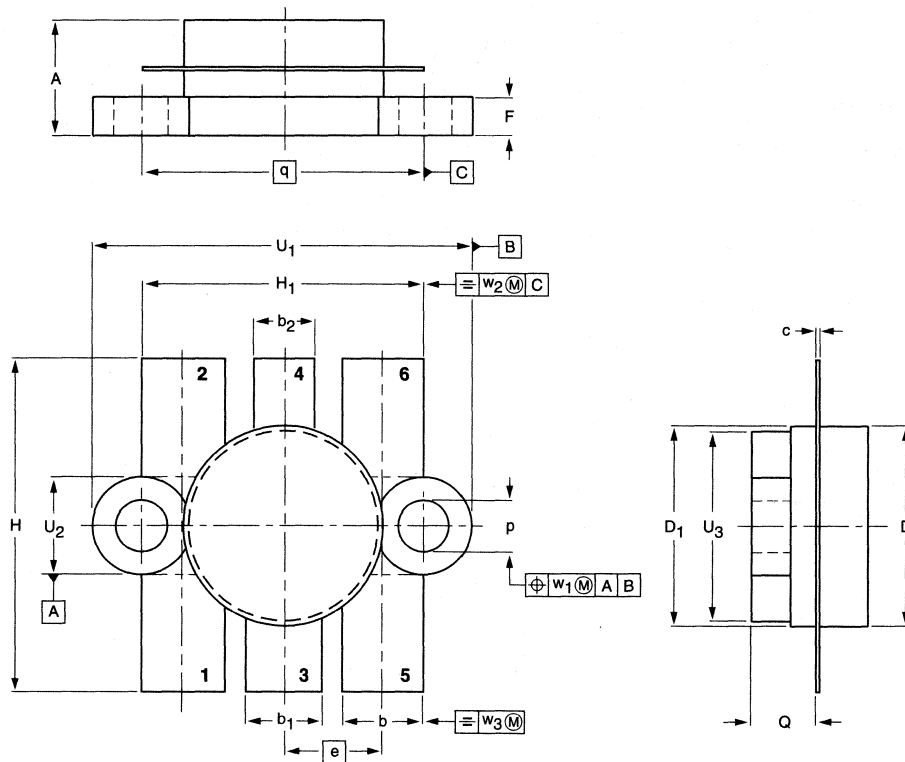
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115T						97-06-05

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 6 leads

SOT119A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	7.39 6.32	5.59 5.33	5.34 5.08	4.07 3.81	0.18 0.07	12.86 12.59	12.83 12.57	6.48	2.54 2.28	22.10 21.08	18.55 18.28	3.31 2.97	4.58 3.98	18.42	25.23 23.95	6.48 6.07	12.76 12.06	0.51	1.02	0.26
inches	0.291 0.249	0.220 0.210	0.210 0.200	0.160 0.150	0.007 0.003	0.505 0.496	0.505 0.495	0.255	0.100 0.090	0.870 0.830	0.730 0.720	0.130 0.117	0.180 0.157	0.725	0.993 0.943	0.255 0.239	0.502 0.475	0.02	0.04	0.01

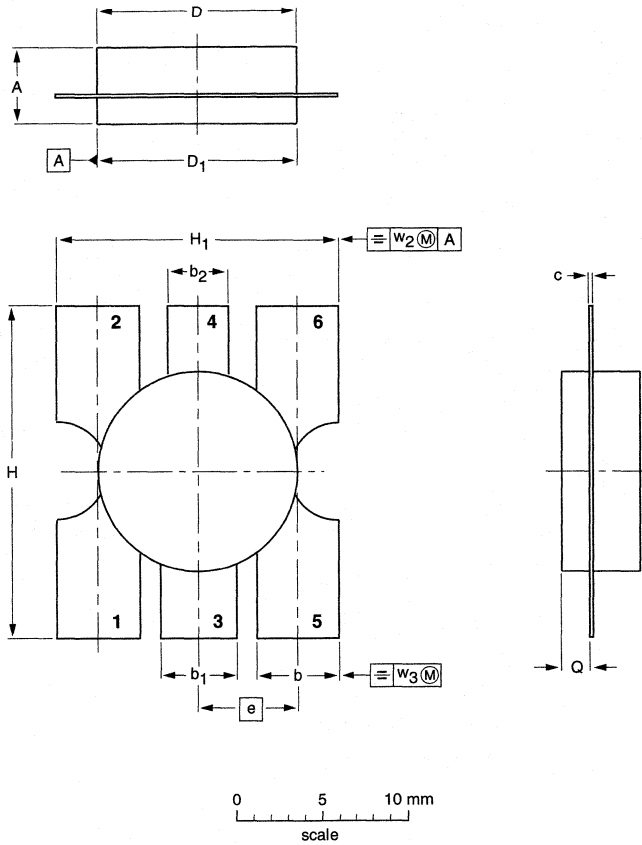
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT119A						97-06-28

Package outlines

Chapter 2

Flangeless ceramic package; 6 leads

SOT119D



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	e	H	H <sub>1</sub>	Q	w <sub>2</sub>	w <sub>3</sub>
mm	4.53 3.70	5.59 5.33	5.34 5.08	4.07 3.81	0.16 0.10	12.86 12.59	12.83 12.57	6.48	21.97 21.20	18.55 18.28	1.71 1.44	0.51	0.26
inches	0.178 0.146	0.220 0.210	0.210 0.200	0.160 0.150	0.006 0.004	0.506 0.496	0.505 0.495	0.255	0.865 0.835	0.730 0.720	0.067 0.057	0.02	0.01

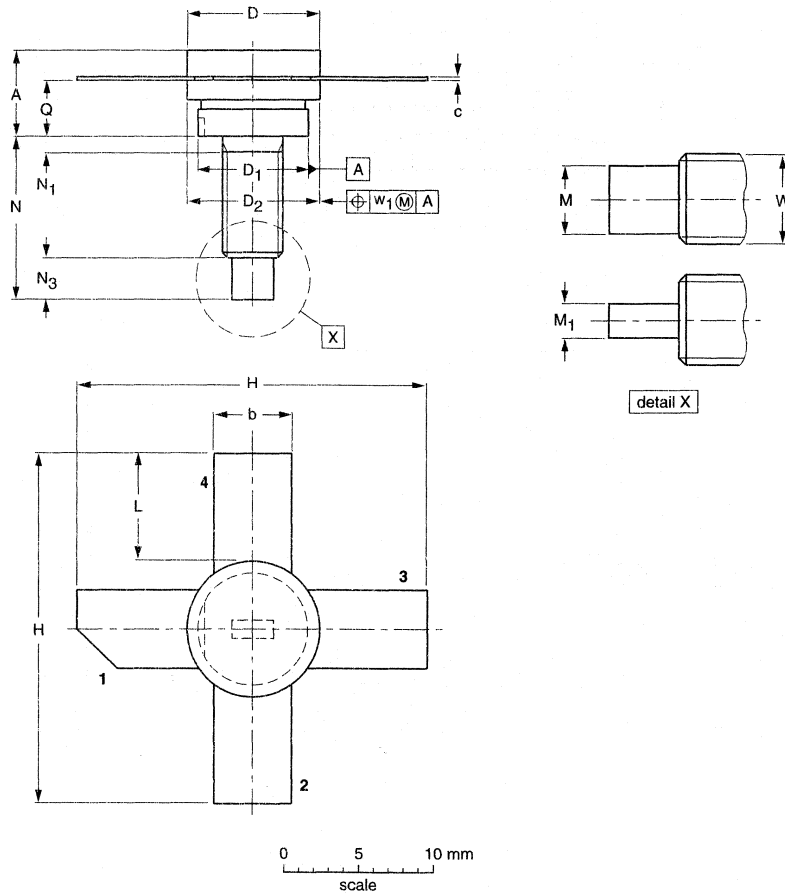
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT119D						97-06-28

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT120A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M	M <sub>1</sub>	N	N <sub>1</sub>	N <sub>3</sub>	Q	W	w <sub>1</sub>
mm	5.97	5.90	0.18	9.73	8.39	9.66	27.44	9.00	3.41	1.66	12.83	1.60	3.31	4.35	8-32 UNC	0.38
	4.74	5.48	0.14	9.47	8.12	9.39	25.78	8.00	2.92	1.39	11.17	0.00	2.54	3.98		
Inches	0.283	0.232	0.007	0.383	0.330	0.380	1.080	0.354	0.134	0.065	0.505	0.063	0.130	0.171	8-32 UNC	0.015
	0.248	0.216	0.004	0.373	0.320	0.370	1.015	0.315	0.115	0.055	0.440	0.000	0.100	0.157		

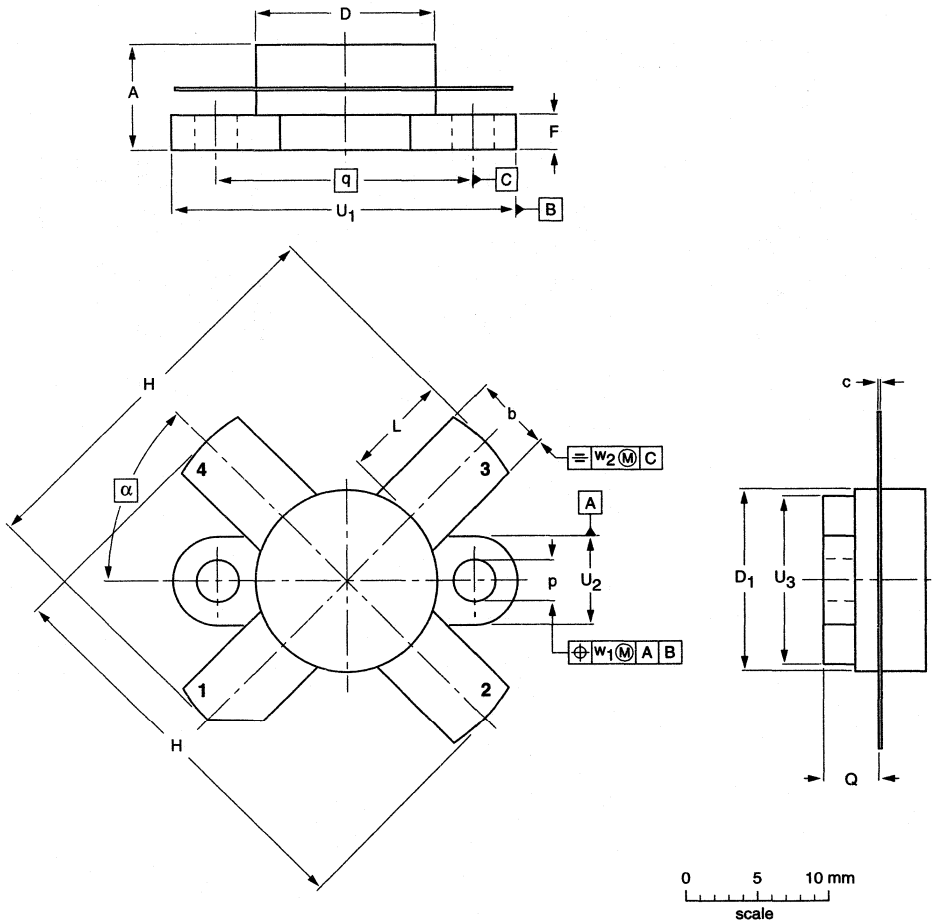
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT120A						97-06-28

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 4 leads

SOT121B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	7.93 6.32	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.51	1.02	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.312 0.249	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.02	0.04	

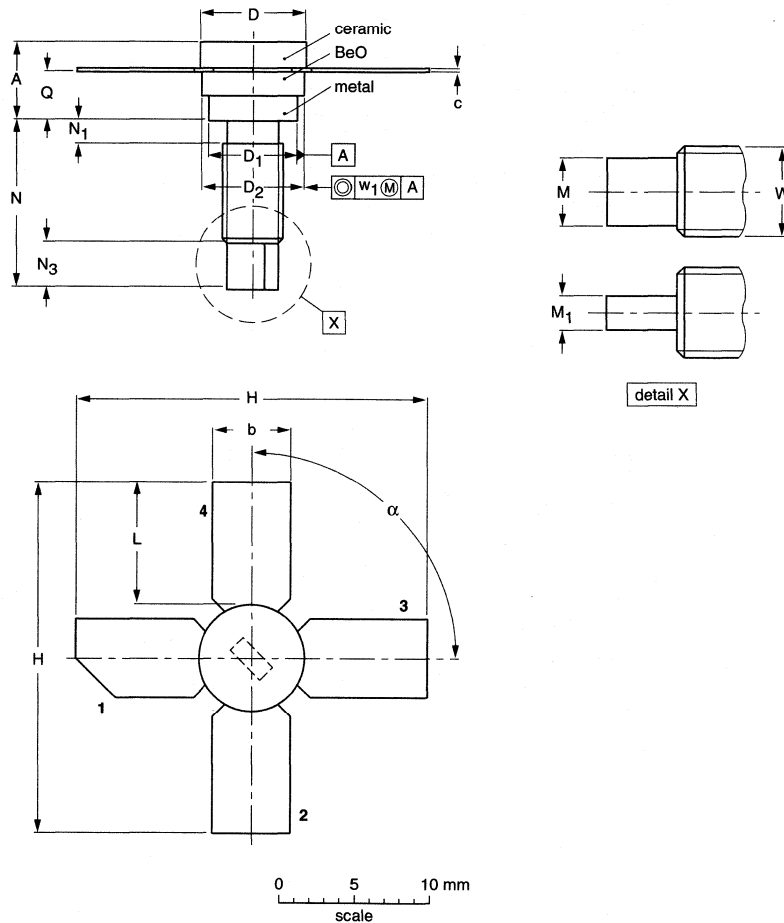
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						97-06-28

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT122A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M <sub>1</sub>	M	N	N <sub>1</sub> max.	N <sub>3</sub>	Q	W	w <sub>1</sub>	α
mm	5.97 4.74	5.85 5.58	0.18 0.14	7.50 7.23	6.48 6.22	7.24 6.93	27.56 25.78	9.91 9.14	3.18 2.66	1.66 1.39	11.82 11.04	1.02	3.86 2.92	3.38 2.74	8-32 UNC	0.381	90°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122A						97-04-18

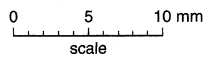
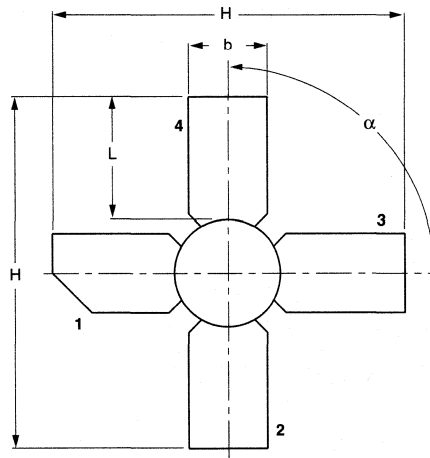
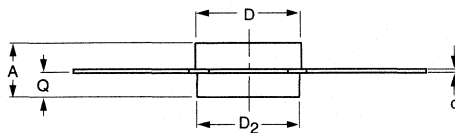


Package outlines

Chapter 2

Studless ceramic package; 4 leads

SOT122D



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	$D_2$	H	L	Q	$\alpha$
mm	4.17 3.27	5.85 5.58	0.18 0.14	7.50 7.23	7.24 6.98	27.56 25.78	9.91 9.14	1.58 1.27	90°

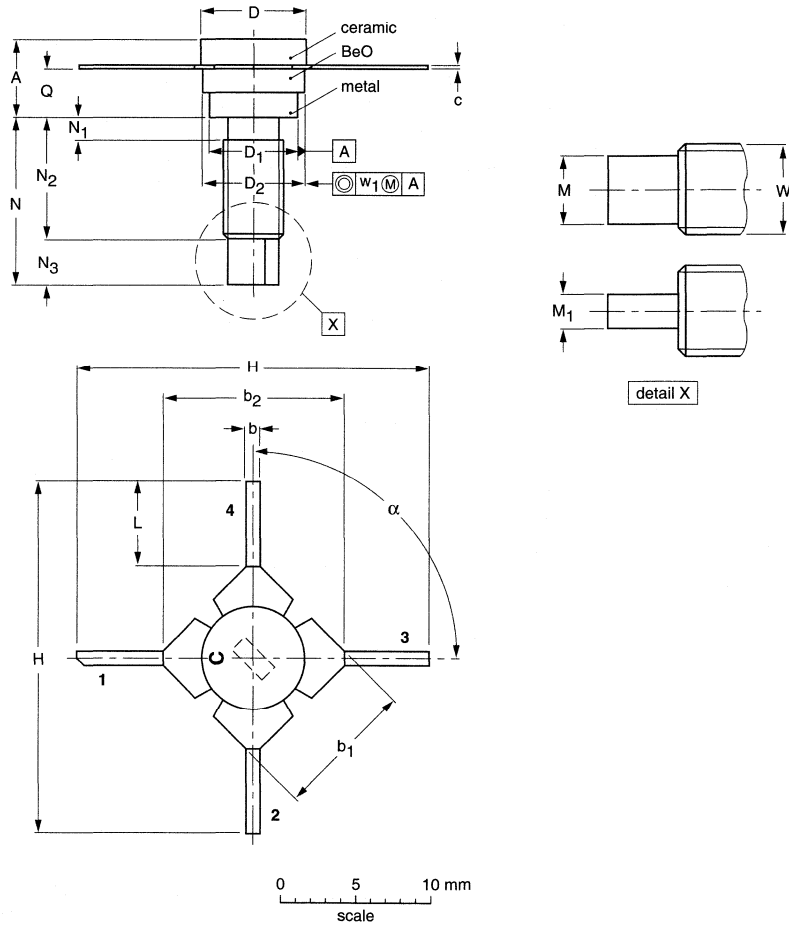
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122D						97-04-18

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT122E



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M	M <sub>1</sub>	N	N <sub>1</sub> max.	N <sub>2</sub>	N <sub>3</sub>	Q	W	w <sub>1</sub>	α
mm	5.97 4.80	1.05 0.73	10.75 10.43	14.25 13.94	0.18 0.14	7.50 7.23	6.46 6.25	7.19 6.93	27.56 25.78	6.84 5.30	3.18 2.92	1.63 1.42	11.82 11.04	1.02	8.89 7.36	3.68 2.92	3.38 2.79	8-32 UNC	0.381	90°

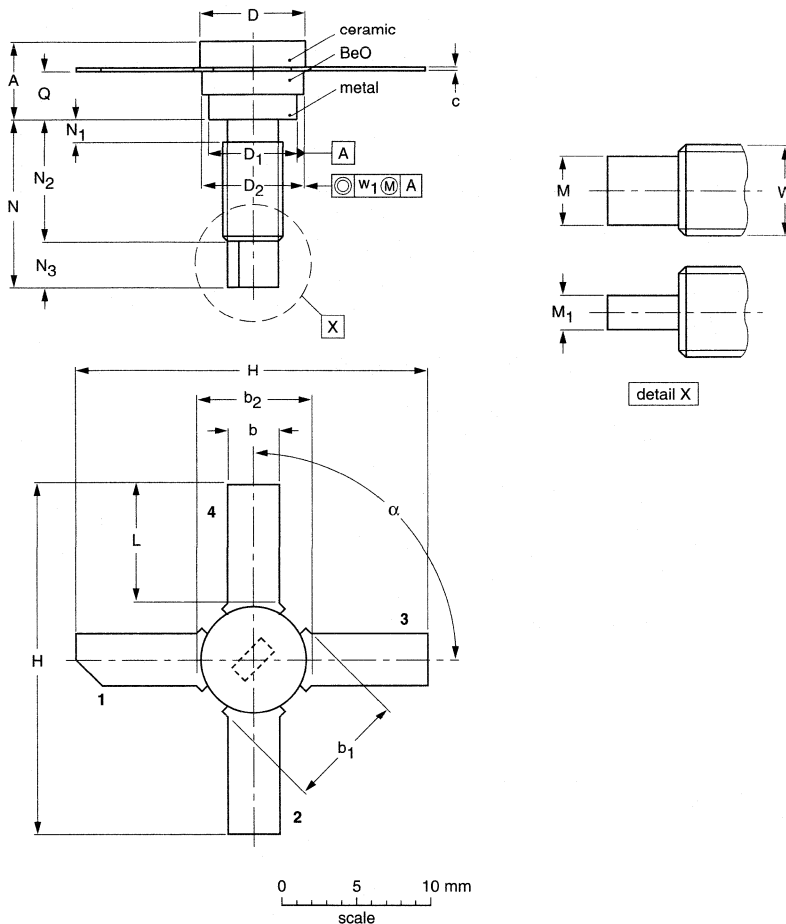
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT122E					97-04-18

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT122F



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	D <sub>2</sub>	H	L	M	M <sub>1</sub>	N	N <sub>1</sub> max.	N <sub>2</sub>	N <sub>3</sub>	Q	W	w <sub>1</sub>	$\alpha$
mm	5.97 4.80	3.92 3.50	8.46 8.15	8.16 7.84	0.18 0.14	7.50 7.23	6.46 6.25	7.19 6.93	27.56 25.78	9.89 8.30	3.18 2.92	1.63 1.42	11.82 11.04	1.02	8.89 7.36	3.68 2.92	3.38 2.79	8-32 UNC	0.381	90°

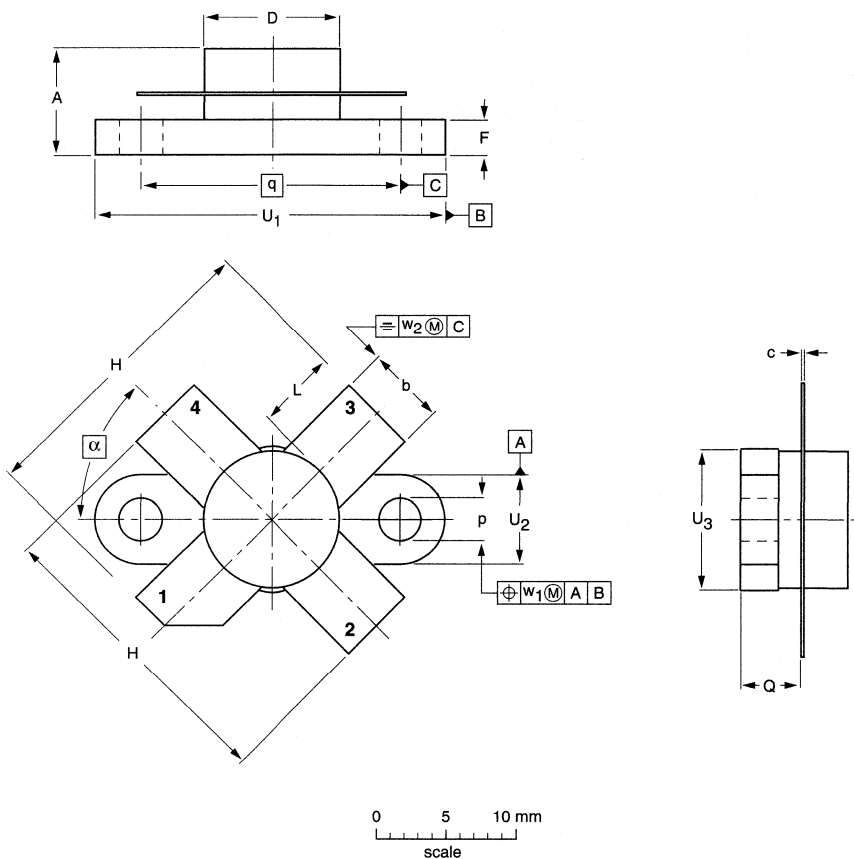
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT122F					97-04-18

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 4 leads

SOT123A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.63 9.42	2.72 2.31	20.71 19.93	5.61 5.16	3.33 3.04	4.63 4.11	18.42	25.15 24.38	6.61 6.09	9.78 9.39	0.51	1.02	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.397 0.371	0.107 0.091	0.815 0.785	0.221 0.203	0.131 0.120	0.182 0.162	0.725	0.99 0.96	0.26 0.24	0.385 0.370	0.02	0.04	

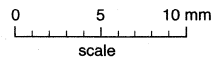
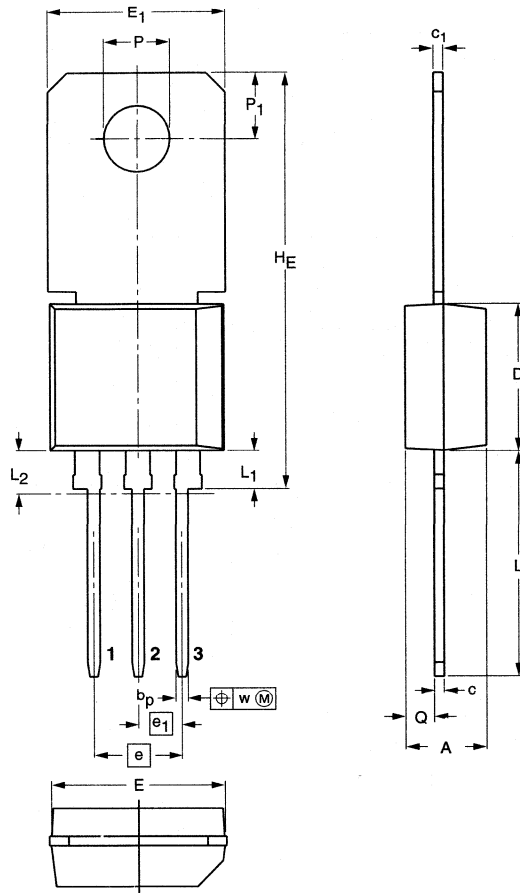
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						97-06-28

Package outlines

Chapter 2

Plastic single-ended leaded (through hole) package; with cooling fin, mountable to heatsink, 1 mounting hole; 3 leads (in-line)

SOT128B



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	c	c <sub>1</sub>	D	E	E <sub>1</sub>	e	e <sub>1</sub>	H <sub>E</sub>	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max	P	P <sub>1</sub>	Q	w
mm	4.6 4.4	0.8 0.6	0.65 0.5	0.56 0.46	8.6 8.4	10.1 9.9	10.4 10.0	5.08	2.54	24.2 23.8	13.3 12.2	2.4 2.0	2.5	3.8 3.6	3.9 3.7	1.7 1.5	0.25

Note

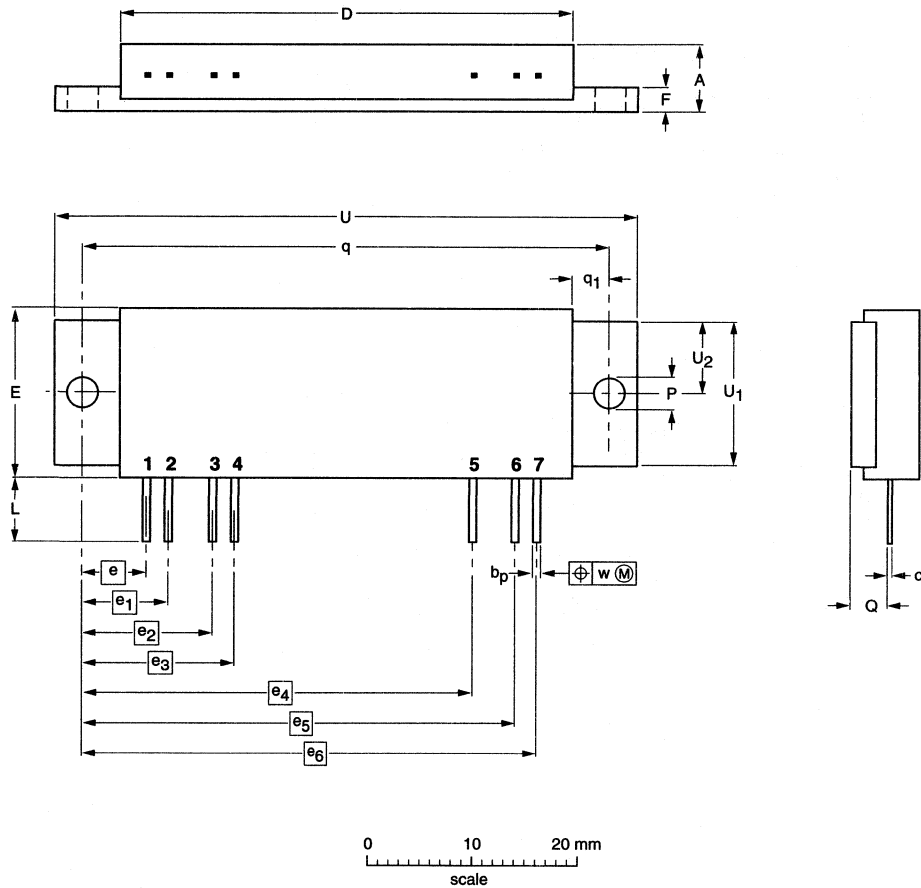
1. Plastic flash allowed within this zone

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT128B		TO-202			97-02-28

Package outlines

Chapter 2

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 7 in-line leads SOT132B



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	D	E	e	$e_1$	$e_2$	$e_3$	$e_4$	$e_5$	$e_6$	F	$L_{max.}$	P	Q	q	$q_1$	U	$U_1$	$U_2$	w
mm	8.1	0.5	0.25	52.5	19.7	6.8	9.3	14.4	17.0	44.9	50.0	52.5	3.3	7.65	3.5	3.7	61.0	4.2	67.5	17.0	8.5	0.2

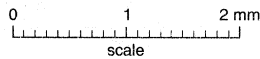
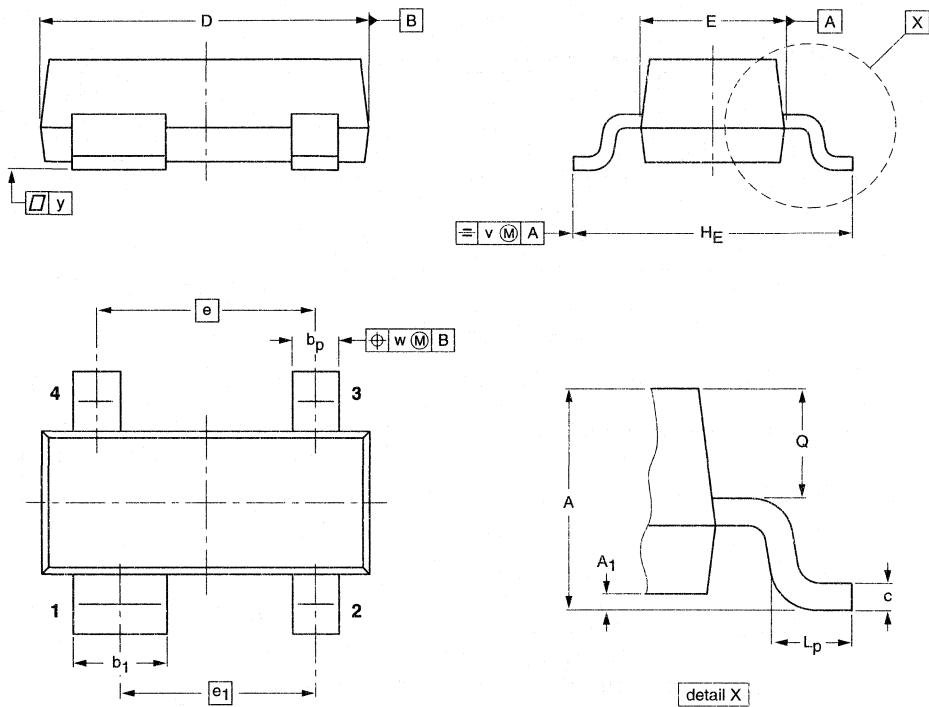
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT132B					97-06-20

Package outlines

Chapter 2

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

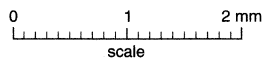
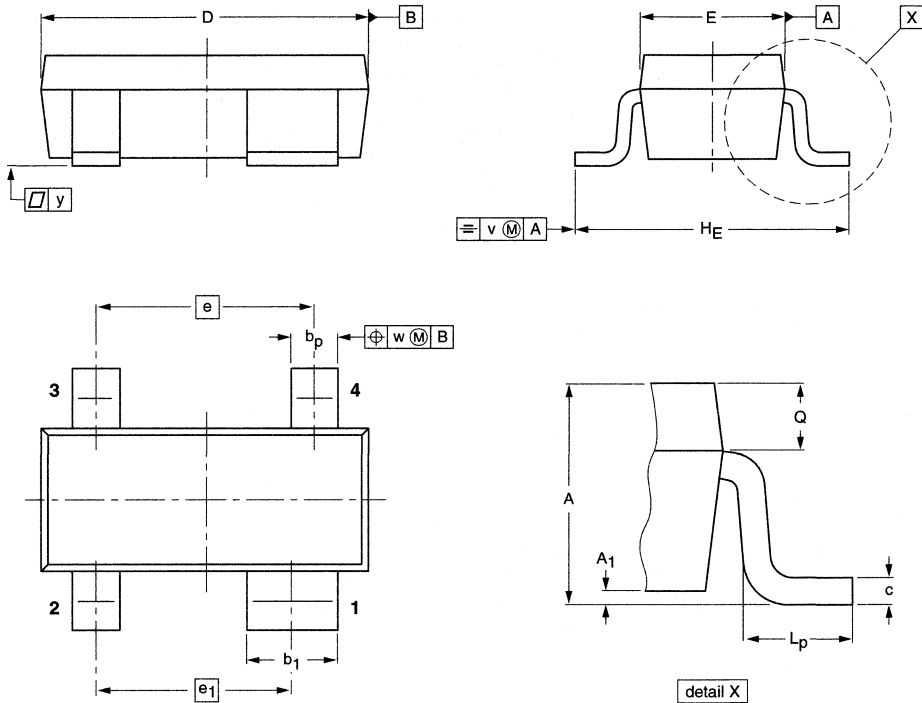
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT143B					97-02-28

Package outlines

Chapter 2

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

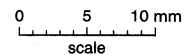
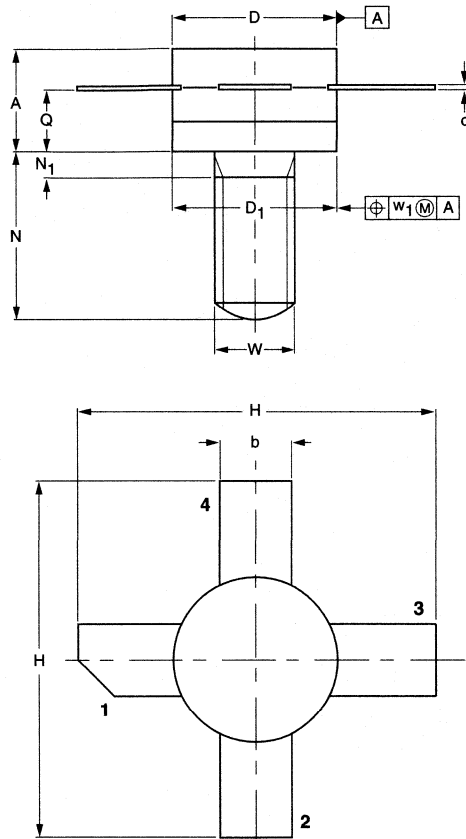


Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT147A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	H	N	N <sub>1</sub> max.	Q	W	w <sub>1</sub>
mm	8.06 7.18	5.82 5.56	0.16 0.10	12.86 12.59	13.34 12.57	28.45 27.43	13.39 12.62	1.40	5.24 4.92	1/4"× 28 UNF	0.51
inches	0.317 0.283	0.229 0.219	0.006 0.004	0.506 0.496	0.525 0.495	1.12 1.08	0.527 0.497	0.055	0.206 0.194		0.02

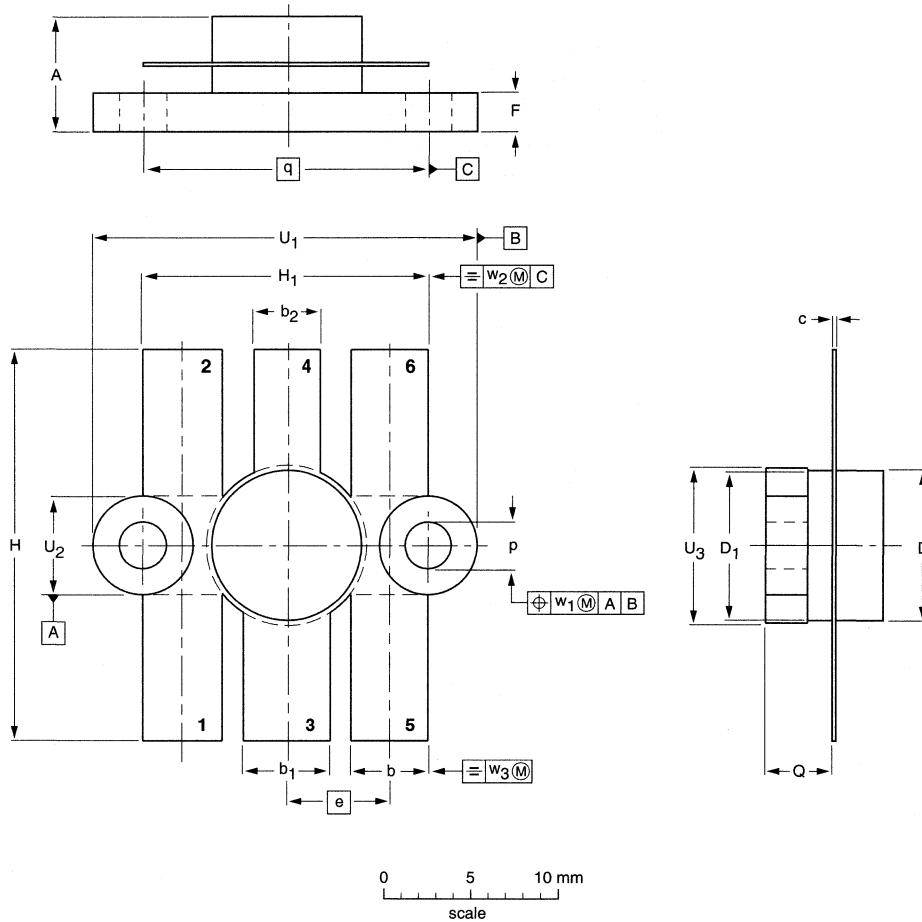
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT147A						97-06-28

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 6 leads

SOT160A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	7.32 6.40	5.21 4.95	5.72 5.46	4.70 4.44	0.16 0.10	9.73 9.47	9.66 9.39	6.60	2.85 2.23	24.39 23.87	18.42 18.16	3.31 3.04	4.50 4.14	18.42	24.90 24.63	6.48 6.22	9.78 9.52	0.51	1.02	0.26
inches	0.288 0.252	0.205 0.195	0.225 0.215	0.185 0.175	0.004 0.006	0.383 0.373	0.380 0.370	0.260	0.112 0.088	0.960 0.940	0.725 0.715	0.130 0.120	0.177 0.163	0.725	0.980 0.970	0.255 0.245	0.385 0.375	0.02	0.04	0.01

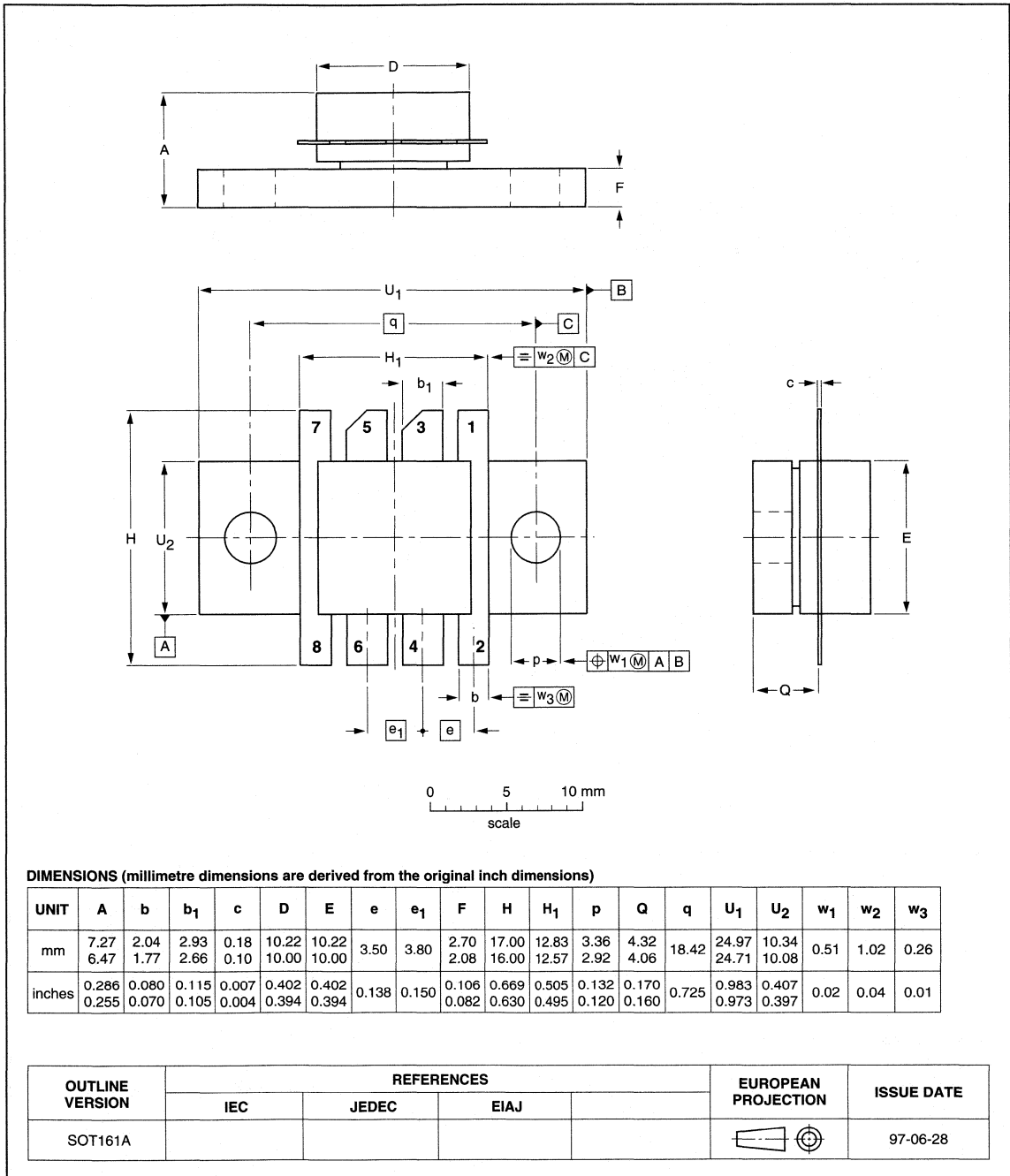
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT160A						97-06-28

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 8 leads

SOT161A

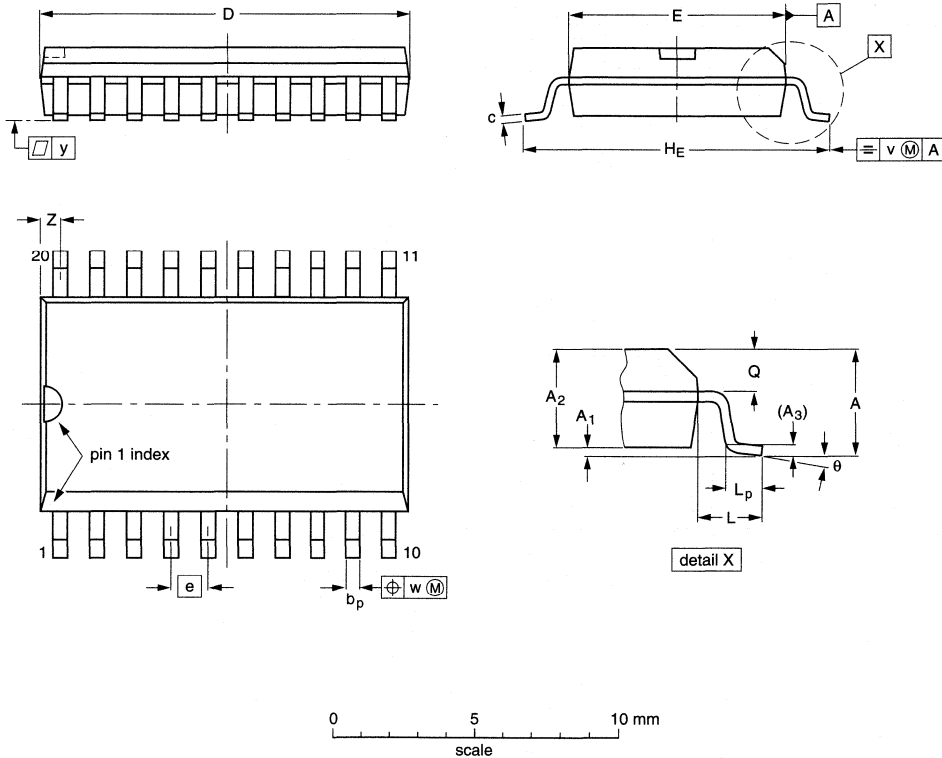


Package outlines

Chapter 2

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

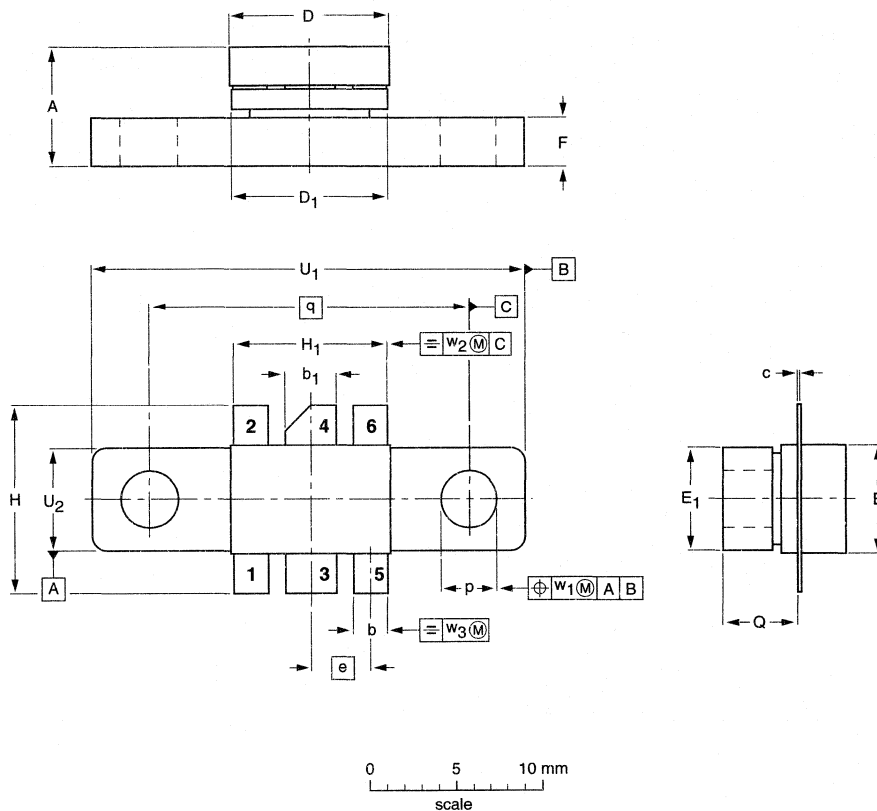
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 6 leads

SOT171A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	6.81 6.07	2.15 1.85	3.20 2.89	0.16 0.07	9.25 9.04	9.30 8.99	5.95 5.74	6.00 5.70	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	6.00 5.70	0.51	1.02	0.26
inches	0.268 0.239	0.085 0.073	0.126 0.114	0.006 0.003	0.364 0.356	0.366 0.354	0.234 0.226	0.236 0.224	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.236 0.224	0.02	0.04	0.01

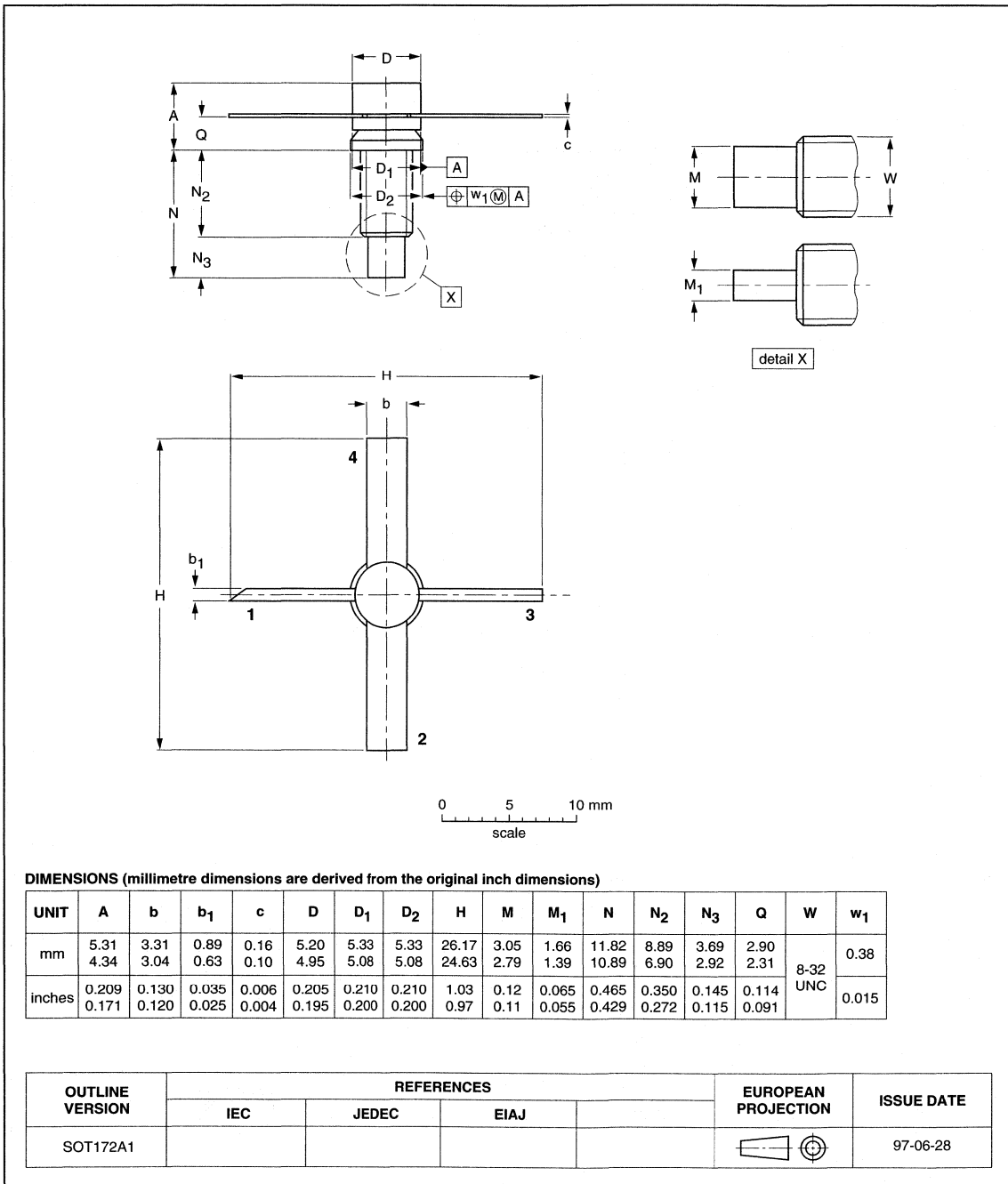
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						97-06-28

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT172A1

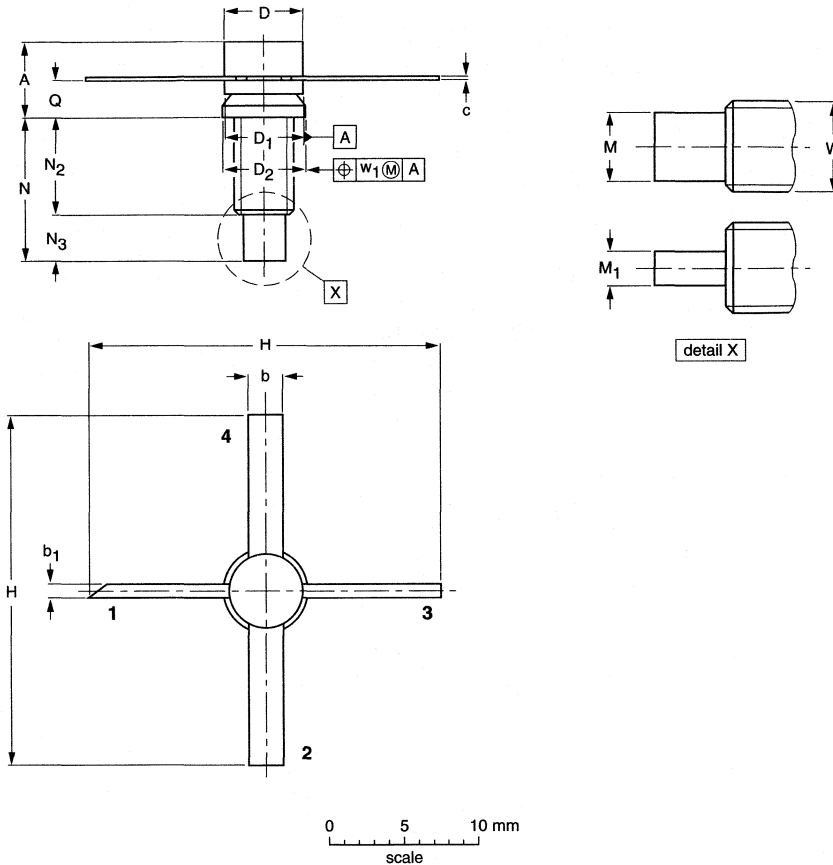


Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT172A2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	D <sub>2</sub>	H	M	M <sub>1</sub>	N	N <sub>2</sub>	N <sub>3</sub>	Q	W	w <sub>1</sub>
mm	5.51 4.45	1.66 1.39	0.89 0.63	0.16 0.10	5.20 4.95	5.33 5.08	5.33 5.08	23.37 22.35	3.05 2.79	1.66 1.39	11.56 11.04	8.38 7.62	3.69 2.92	2.95 2.43	8-32 UNC	0.38
inches	0.217 0.175	0.065 0.055	0.035 0.025	0.006 0.004	0.205 0.195	0.210 0.200	0.210 0.200	0.92 0.88	0.12 0.11	0.065 0.055	0.465 0.435	0.33 0.30	0.145 0.115	0.116 0.096		0.015

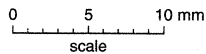
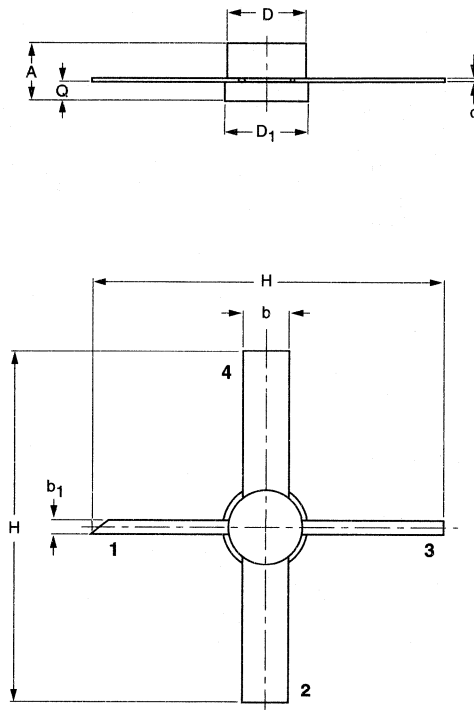
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172A2						97-06-28

Package outlines

Chapter 2

Studless ceramic package; 4 leads

SOT172D



**DIMENSIONS** (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	H	Q
mm	3.71 2.89	3.31 3.04	0.89 0.63	0.16 0.10	5.20 4.95	5.33 5.08	26.17 24.63	1.15 0.88
inches	0.146 0.114	0.13 0.12	0.035 0.025	0.006 0.004	0.205 0.195	0.210 0.200	1.03 0.97	0.045 0.035

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172D						97-06-28

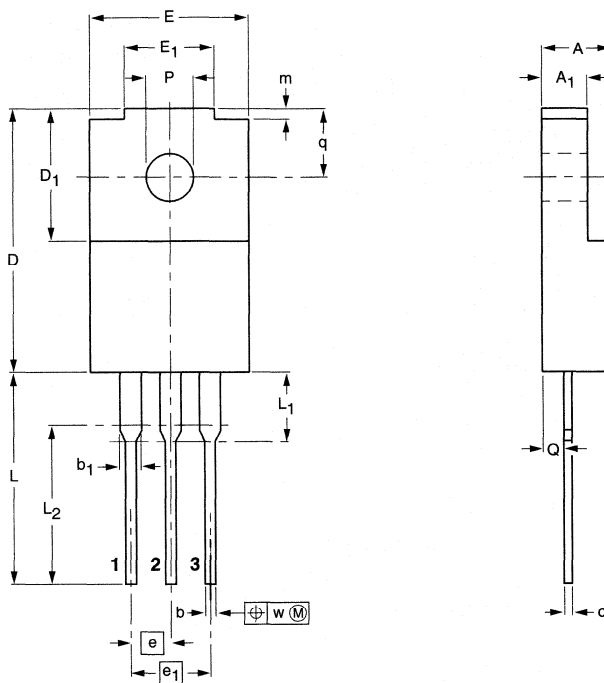


Package outlines

Chapter 2

Plastic single-ended package; isolated heatsink mounted;  
1 mounting hole; 3 lead TO-220 exposed tabs

SOT186



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>	L <sub>2</sub>	m	P	Q	q	w
mm	4.4 4.0	2.9 2.5	0.9 0.7	1.5 1.3	0.55 0.38	17.0 16.4	7.9 7.5	10.2 9.6	5.7 5.3	2.54	5.08	14.3 13.5	4.8 4.0	10	0.9 0.5	3.2 3.0	1.4 1.2	4.4 4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

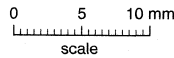
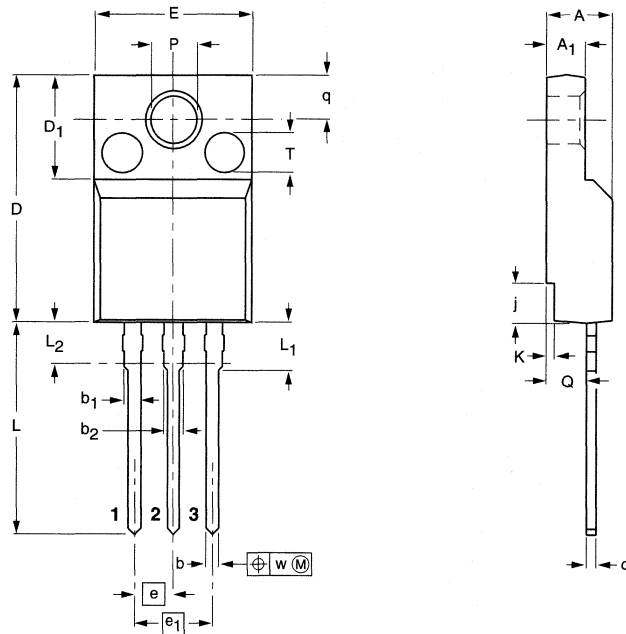
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186		TO-220				97-06-11

Package outlines

Chapter 2

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	e <sub>1</sub>	j	K	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	Q	q	T <sup>(2)</sup>	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

- Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
- Both recesses are  $\varnothing 2.5 \times 0.8$  max. depth

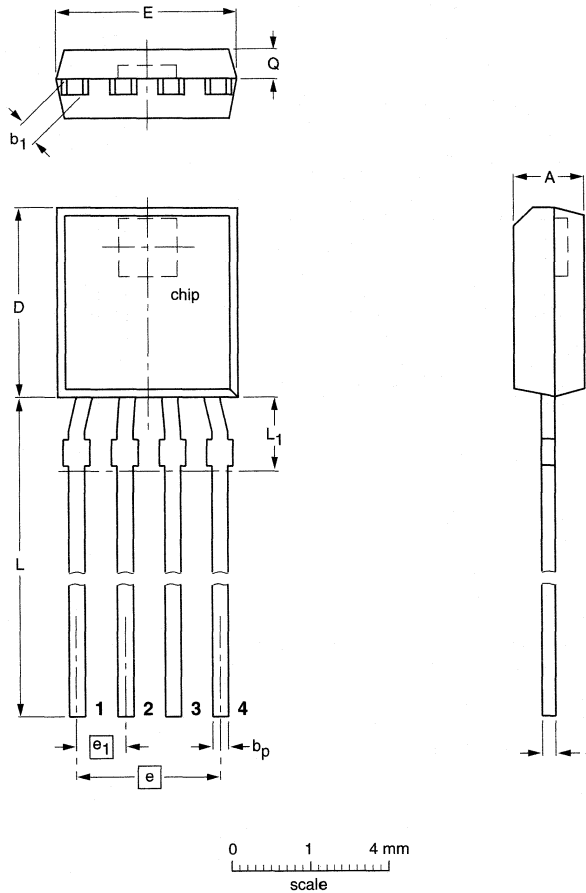
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		TO-220				97-06-11

Package outlines

Chapter 2

Plastic single-ended flat package; 4 in-line leads

SOT195



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.	Q
mm	1.8 1.6	0.48 0.40	0.7 0.5	0.45 0.39	5.2 5.0	4.8 4.4	3.75	1.25	14.5 12.7	2	0.8 0.7

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

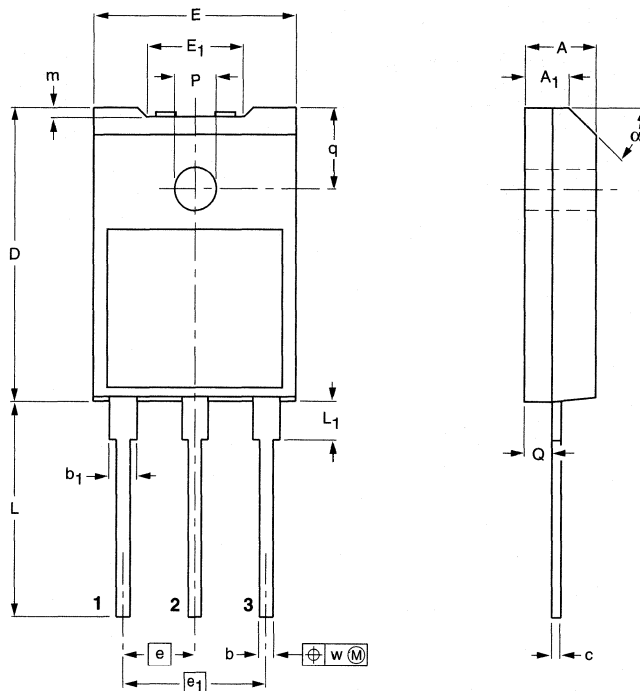
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT195					97-06-02

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)

SOT199



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	E	E <sub>1</sub>	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup>	m	P	Q	q	w	α
mm	5.2 4.8	3.4 3.0	1.2 1.0	2.1 1.9	0.6 0.5	21.5 20.5	15.3 14.7	7.8 6.8	5.45	10.9	16.5 15.7	3.7 3.3	0.8 0.6	3.3 3.1	2.1 1.9	6.2 5.8	0.4	45°

Note

1. Terminals in this zone are not tinned.

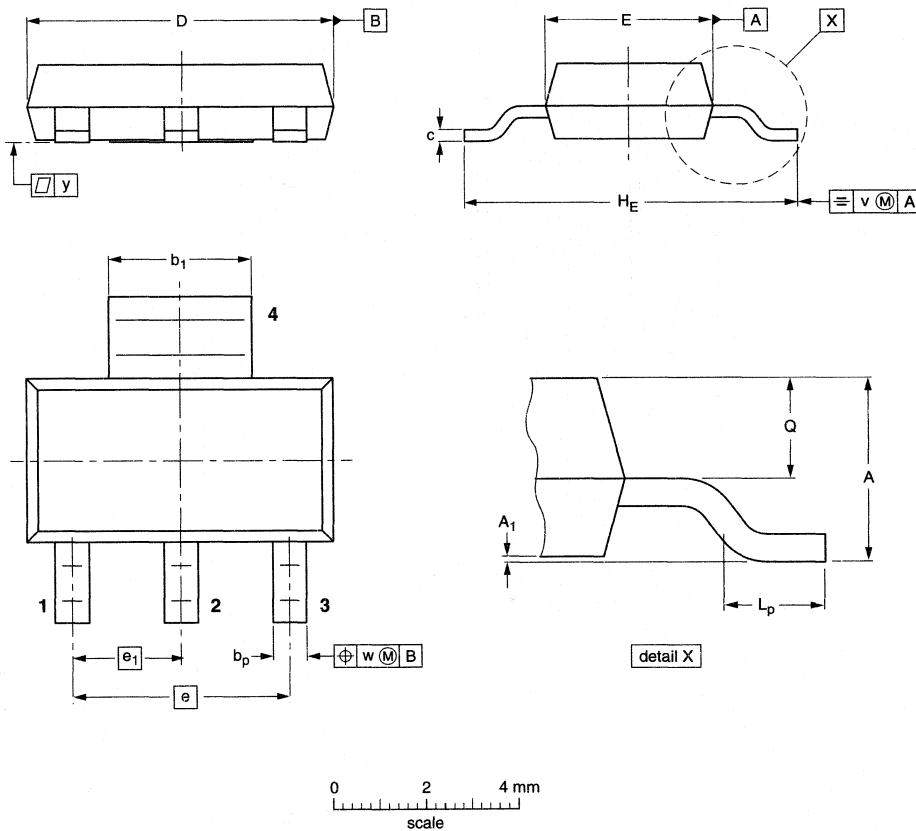
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT199						97-06-27

Package outlines

Chapter 2

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8	0.10	0.80	3.1	0.32	6.7	3.7	4.6	2.3	7.3	1.1	0.95	0.2	0.1	0.1
	1.5	0.01	0.60	2.9	0.22	6.3	3.3			6.7	0.7	0.85			

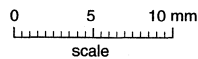
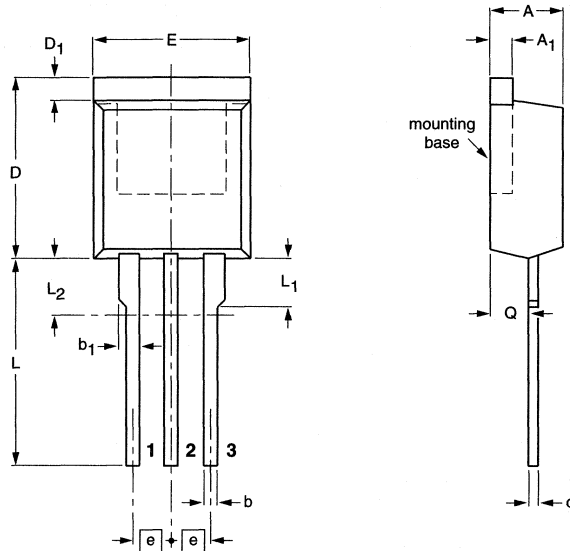
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

Package outlines

Chapter 2

Plastic single-ended package; 3 lead low-profile TO-220

SOT226



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	2.6 2.2

Note

1. Terminals in this zone are not tinned.

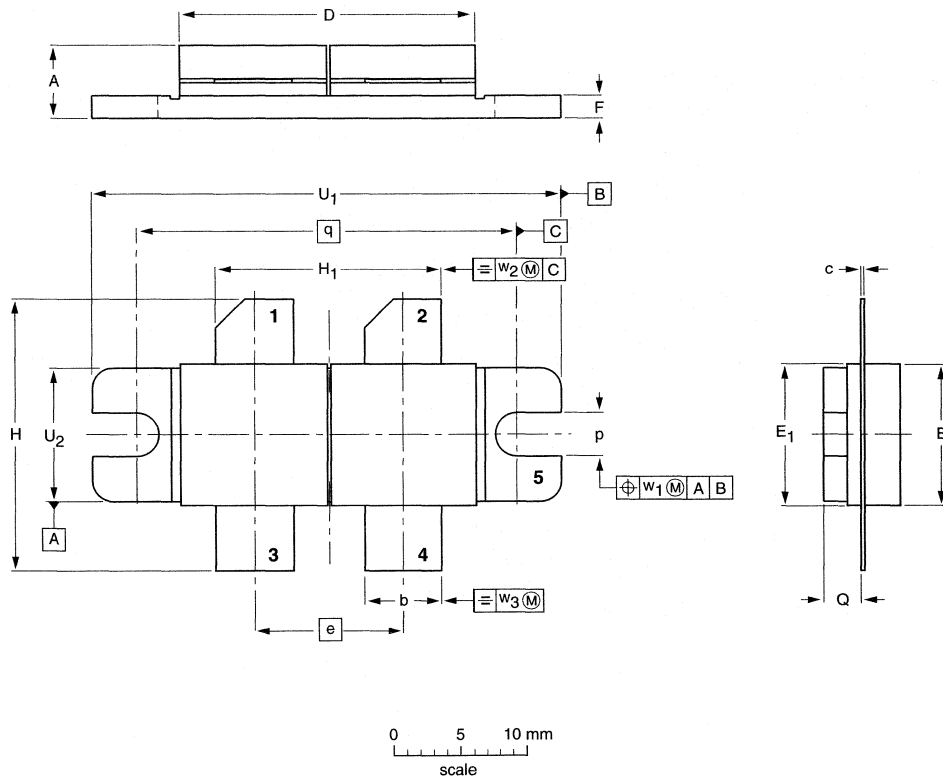
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT226		low-profile TO-220			97-06-11

Package outlines

Chapter 2

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	5.77 5.00	5.85 5.58	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	20.58 20.06	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.865 0.855	0.435	0.404 0.396	0.405 0.395	0.070 0.060	0.81 0.79	0.67 0.65	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

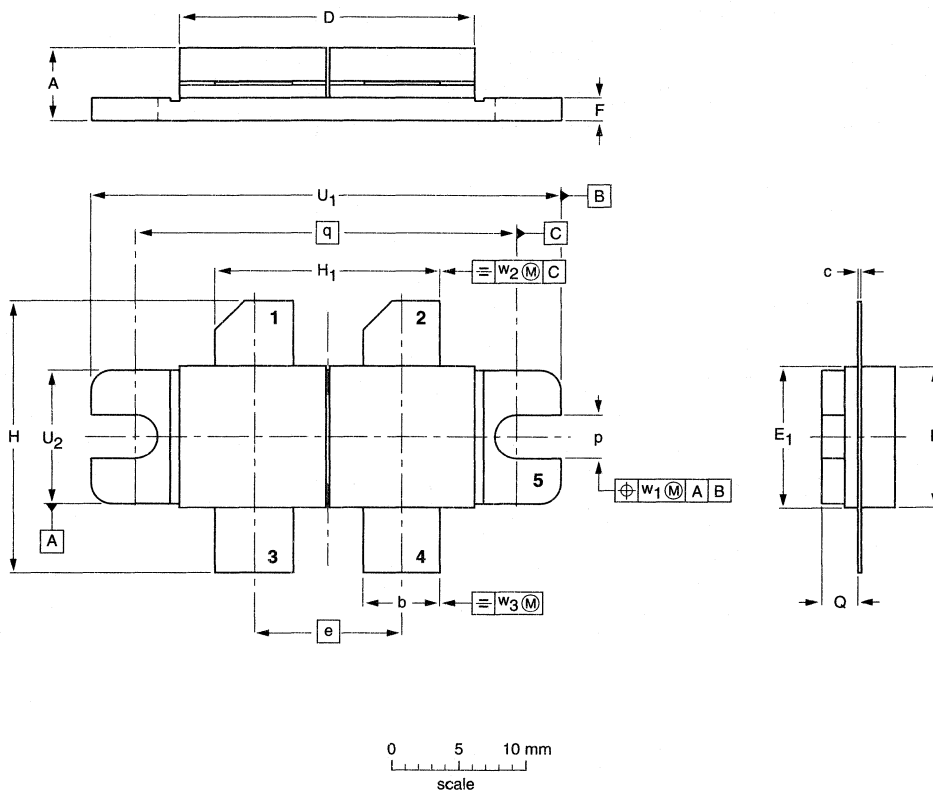
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						97-06-28

Package outlines

Chapter 2

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	5.39 4.62	5.85 5.58	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	20.58 20.06	17.02 16.51	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.212 0.182	0.230 0.220	0.006 0.004	0.865 0.855	0.435	0.404 0.395	0.405 0.396	0.070 0.060	0.81 0.79	0.67 0.65	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A2						97-06-28

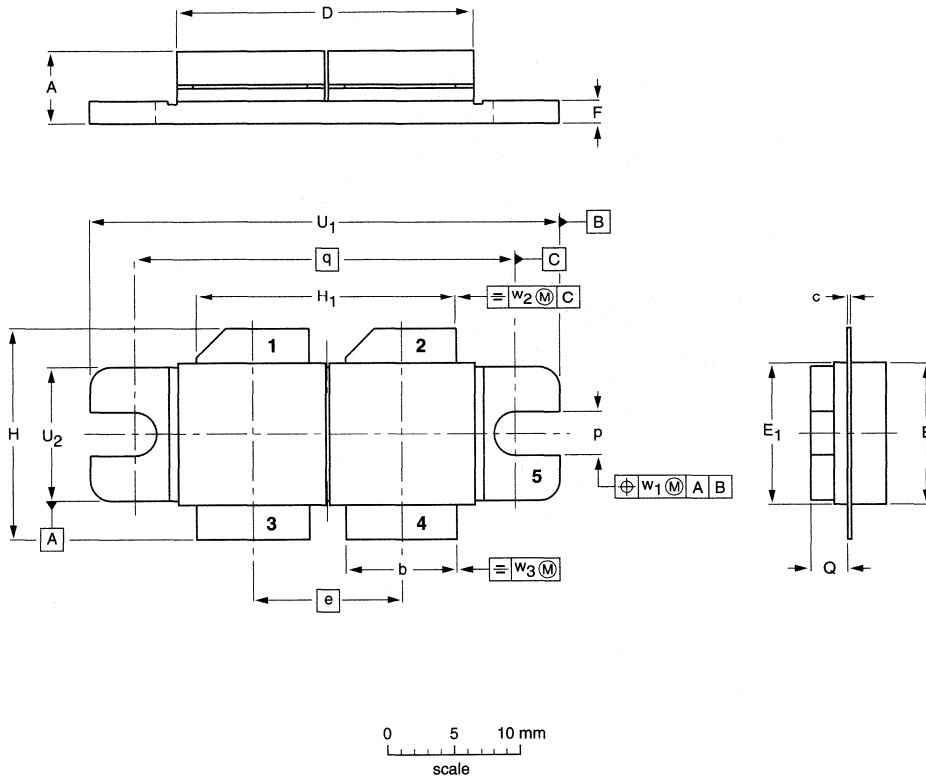


Package outlines

Chapter 2

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	5.39 4.62	8.51 8.25	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	15.50 14.98	19.69 19.17	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.212 0.182	0.335 0.325	0.006 0.004	0.865 0.855	0.435	0.404 0.396	0.405 0.395	0.070 0.060	0.61 0.59	0.775 0.755	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

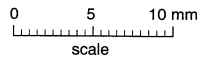
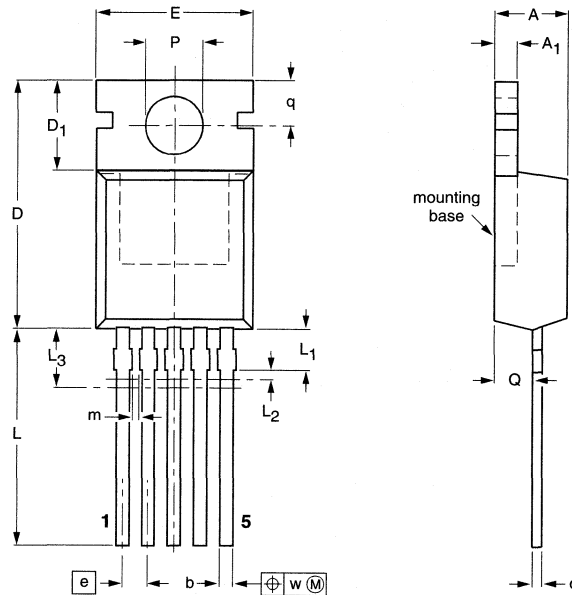
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262B						97-06-28

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220

SOT263



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> <sup>(1)</sup>	L <sub>2</sub> <sup>(2)</sup>	L <sub>3</sub> <sup>(3)</sup> max.	m	P	q	Q	w
mm	4.5	1.39	0.9	0.7	15.8	6.4	10.3		15.0	2.4	0.5	3.5	0.8	3.8	3.0	2.6	
	4.1	1.27	0.7	0.4	15.2	5.9	9.7	1.7	13.5	1.6		0.6	3.6	2.7	2.2	0.4	

**Notes**

1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminals in this zone are not tinned.

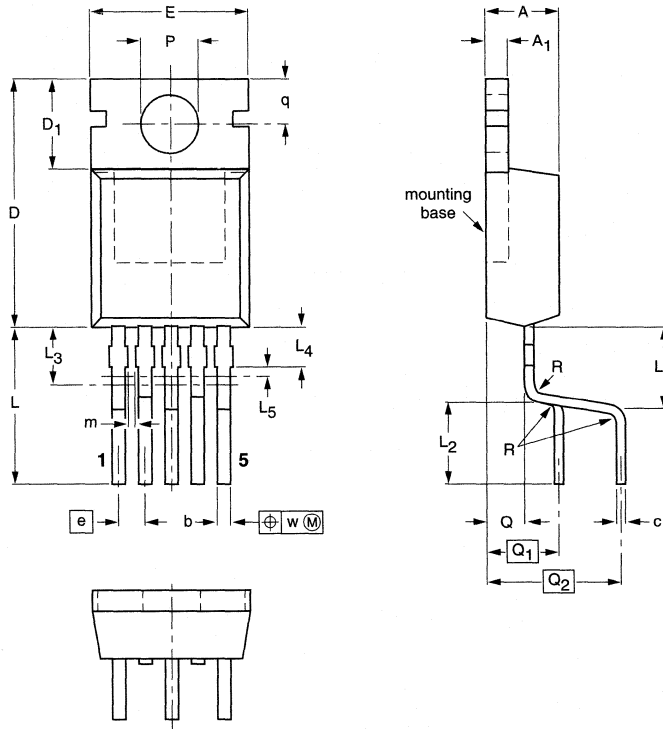
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT263		5-lead TO-220			97-06-11

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole;  
5-lead TO-220 lead form option

SOT263-01



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub>	L <sub>2</sub>	L <sub>3</sub> <sup>(1)</sup> max.	L <sub>4</sub> <sup>(2)</sup>	L <sub>5</sub> <sup>(3)</sup> max.	m	P	q	Q	Q <sub>1</sub>	Q <sub>2</sub>	R	w
mm	4.5	1.39	0.90	0.7	15.8	6.4	10.3	1.7	9.8	5.9	5.2	3.5	2.4	0.5	0.8	3.8	3.0	2.0	4.5	8.2	0.5	0.4
	4.1	1.27	0.75	0.4	15.2	5.9	9.7		9.7	5.3	5.0		1.6		0.6	3.6	2.7					

Notes

1. Terminals in this zone are not tinned.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminal dimensions are uncontrolled in this zone.

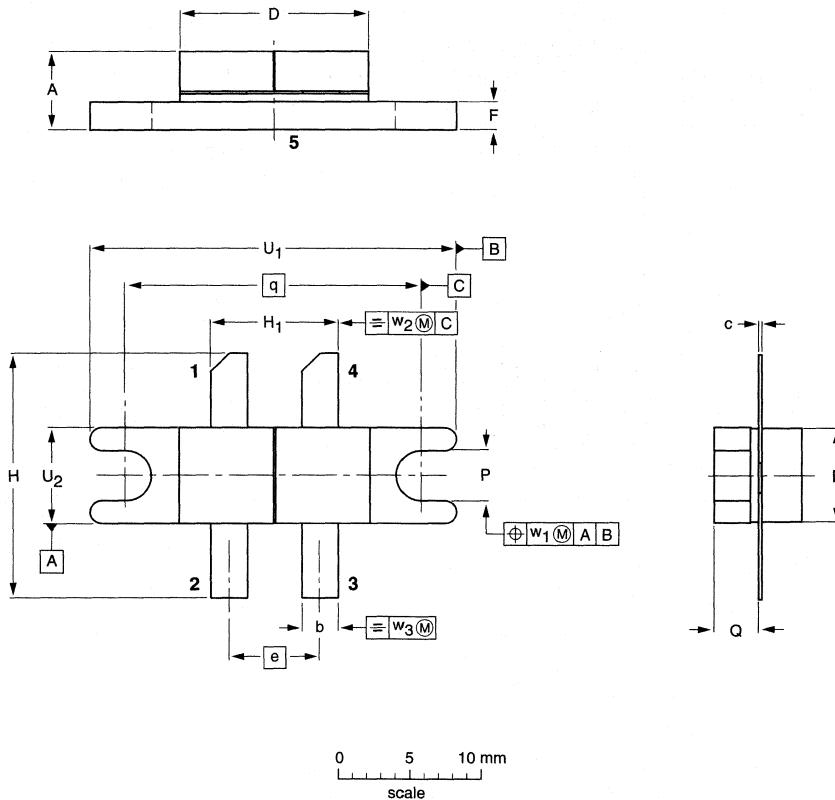
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT263-01		5-lead (option) TO-220			97-06-11

Package outlines

Chapter 2

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT268A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.51	1.02	0.26
inches	0.193 0.165	0.065 0.055	0.005 0.003	0.510 0.490	0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.02	0.04	0.01

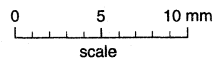
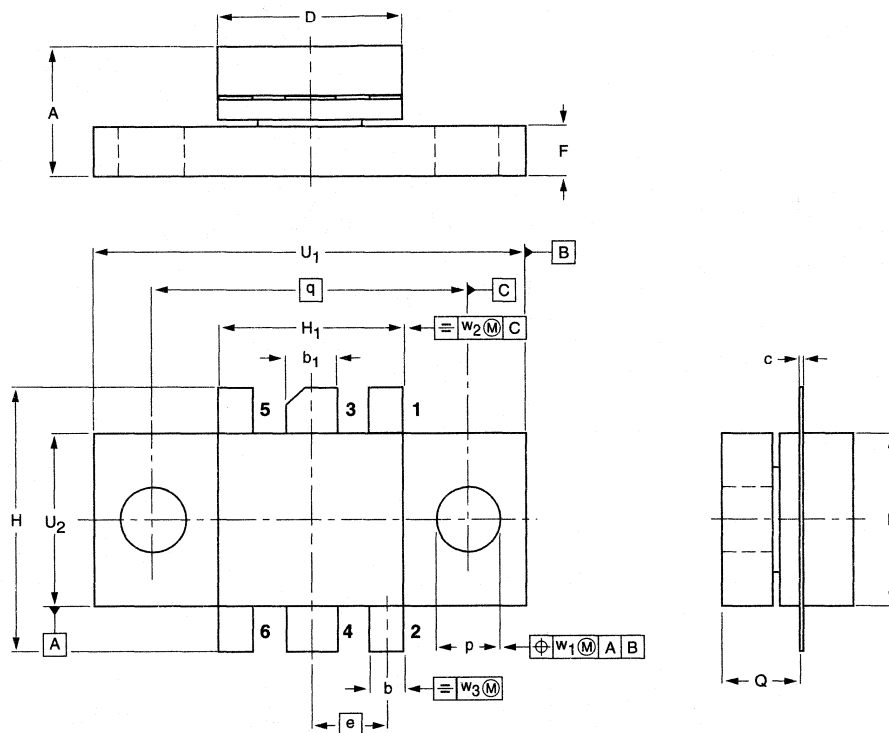
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT268A						97-06-28

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 6 leads

SOT273A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

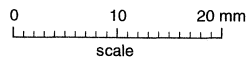
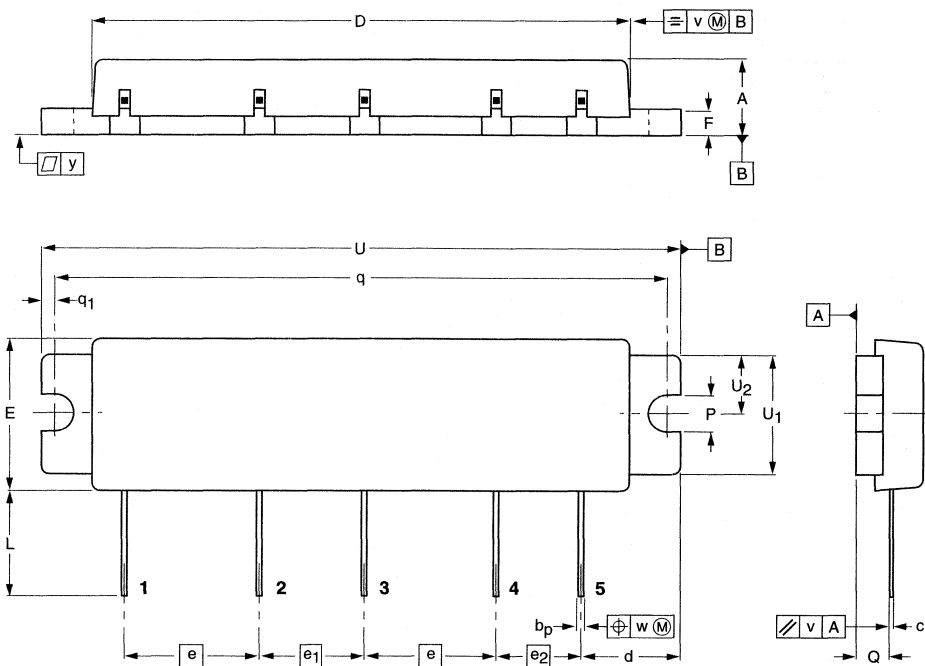
UNIT	A	b	b <sub>1</sub>	c	D	E	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	7.45 7.27	2.42 1.80	3.18 2.92	0.16 0.10	10.93 10.66	10.29 10.03	4.35	3.05 2.54	15.75 14.73	10.93 10.66	3.31 3.04	4.35 4.03	18.42	24.90 24.63	10.29 10.03	0.51	1.02	0.25
inches	0.286 0.254	0.095 0.071	0.125 0.115	0.006 0.004	0.430 0.420	0.405 0.395	0.171	0.120 0.100	0.62 0.58	0.43 0.42	0.130 0.120	0.171 0.159	0.725	0.98 0.97	0.405 0.395	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT273A						97-06-28

Package outlines

Chapter 2

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 5 in-line leads SOT278A



DIMENSIONS (mm are the original dimensions)

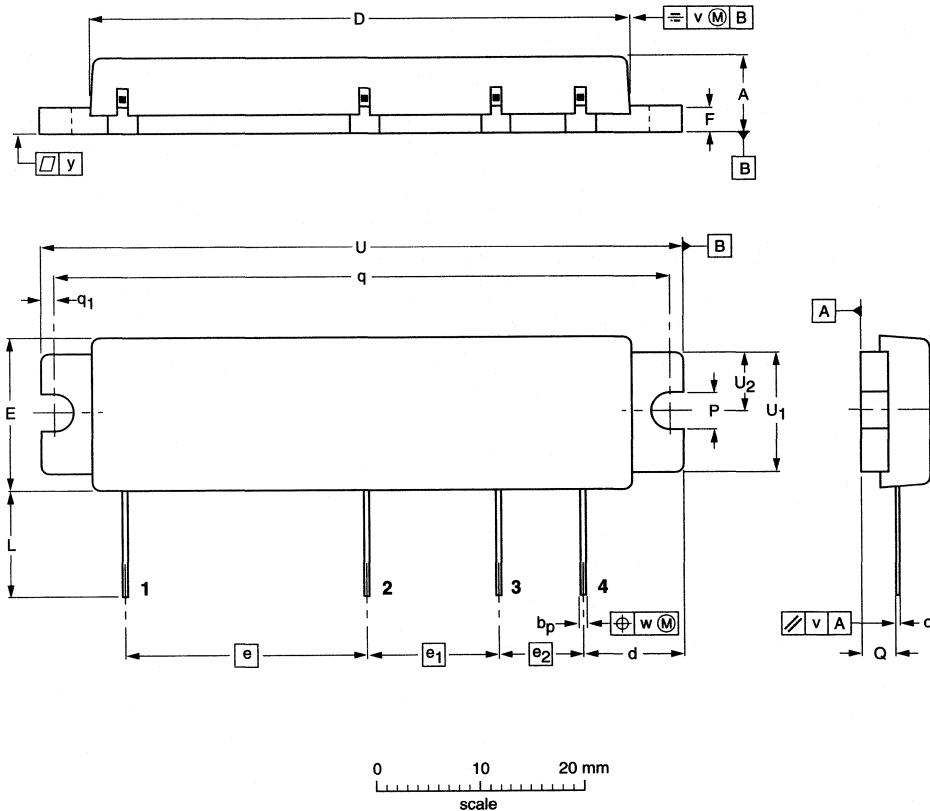
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mm	7.0	0.58 0.45	0.3 0.2	50.4	9.5 8.5	14	12.7	10.16	7.62	2.4 2.2	7.2	3.3 3.1	3.4 3.0	57.6 57.4	1.6 1.4	60.7	11.1 10.9	5.6 5.4	0.5	0.25	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT278A						97-06-20

Package outlines

Chapter 2

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads SOT278B



DIMENSIONS (mm are the original dimensions)

UNIT	A max	b <sub>p</sub>	c	D max	d	E max	e	e <sub>1</sub>	e <sub>2</sub>	F	L min	P	Q	q	q <sub>1</sub>	U max	U <sub>1</sub>	U <sub>2</sub>	v	w	y
mm	7.0	0.58 0.45	0.3 0.2	50.4	9.5 8.5	14	22.86	12.7	7.62	2.4 2.2	7.2	3.3 3.1	3.4 3.0	57.6 57.4	1.6 1.4	60.7	11.1 10.9	5.6 5.4	0.5	0.25	0.1

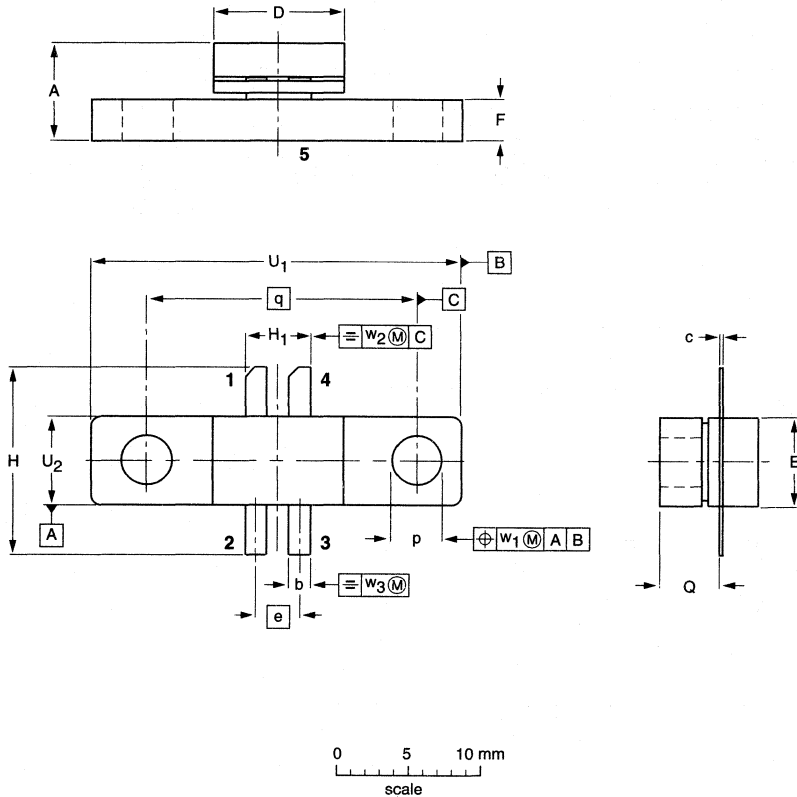
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT278B						97-06-20

Package outlines

Chapter 2

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT279A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	6.84 6.01	1.66 1.39	0.16 0.10	9.28 9.01	5.97 5.71	3.05	3.05 2.54	12.96 11.93	4.96 4.19	3.48 3.22	4.35 4.03	18.42	24.90 24.63	5.97 5.71	0.51	1.02	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.365 0.355	0.235 0.225	0.12	0.120 0.100	0.51 0.47	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.98 0.97	0.235 0.225	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT279A						97-06-28

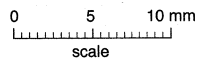
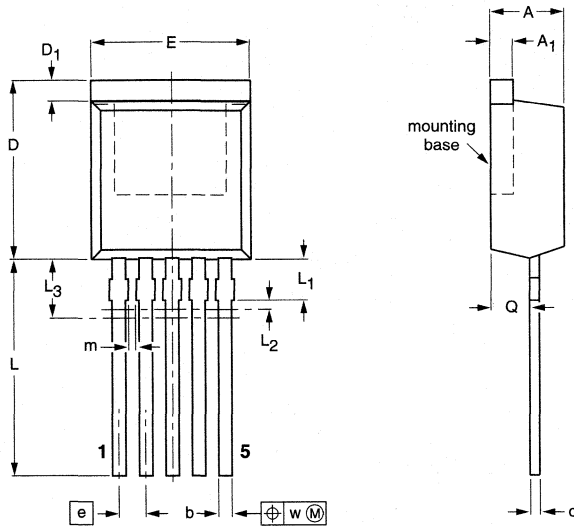


Package outlines

Chapter 2

Plastic single-ended package; 5-lead low-profile TO-220

SOT281



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> ( <sup>1</sup> )	L <sub>2</sub> ( <sup>2</sup> )	L <sub>3</sub> ( <sup>3</sup> ) max.	m	Q	w
mm	4.5 4.1	1.39 1.27	0.9 0.7	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	1.7	15.0 13.5	2.4 1.6	0.5	3.5	0.8 0.6	2.6 2.2	0.4

Notes

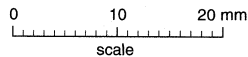
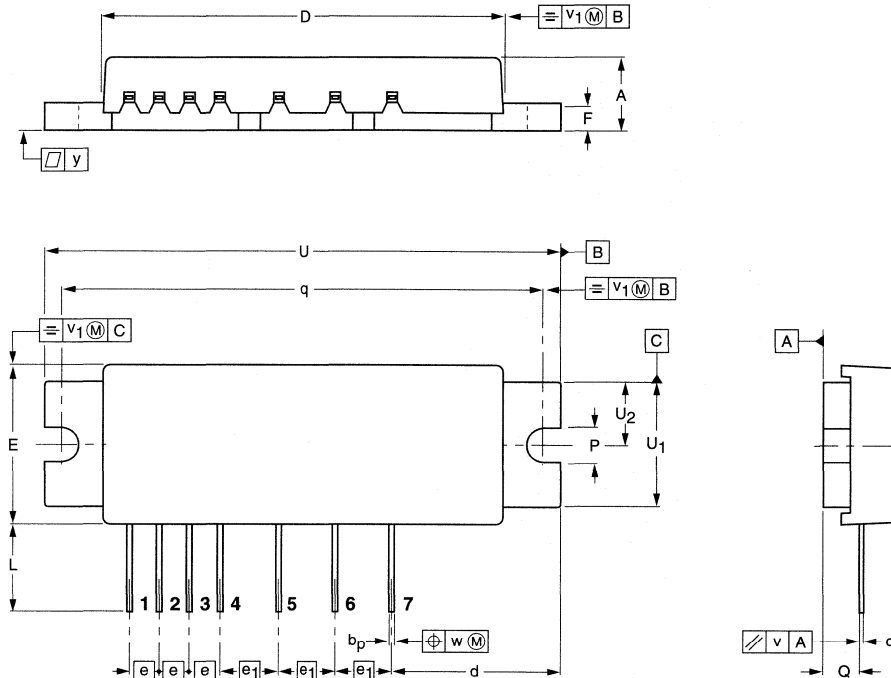
1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT281		low-profile 5-lead TO-220				97-06-11

Package outlines

Chapter 2

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 7 in-line leads SOT288D



DIMENSIONS (mm are the original dimensions)

UNIT	A	$b_p$	c	$D_{max}$	d	$E_{max}$	e	$e_1$	F	L	P	Q	q	$U_{max}$	$U_{1max}$	$U_2$	v	$v_1$	w	y
mm	6.7 6.2	0.56 0.46	0.3 0.2	35.3	14.98 14.78	14	2.54	5.08	2.55 2.45	7.6 7.4	3.2 3.0	3.3 3.1	42.0 41.8	45.3	11.8	5.6 5.4	0.3	0.2	0.25	0.1

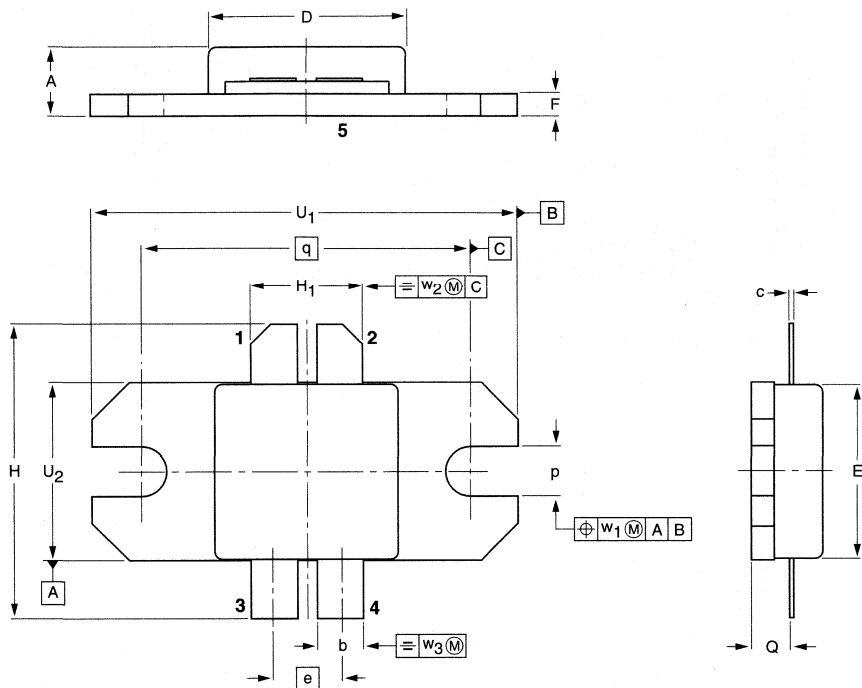
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT288D						97-06-20

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 4 leads

SOT289A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H <sub>1</sub>	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
mm	4.65 3.92	3.33 3.07	0.10 0.05	13.10 12.90	11.53 11.33	4.60	1.65 1.40	19.81 19.05	4.85 4.34	3.43 3.17	2.31 2.06	21.44	28.07 27.81	11.81 11.56	0.51	1.02	0.25
inches	0.183 0.154	0.131 0.121	0.004 0.002	0.516 0.508	0.454 0.446	0.181	0.065 0.055	0.780 0.750	0.191 0.171	0.135 0.125	0.091 0.081	0.844	1.105 1.095	0.465 0.455	0.02	0.04	0.01

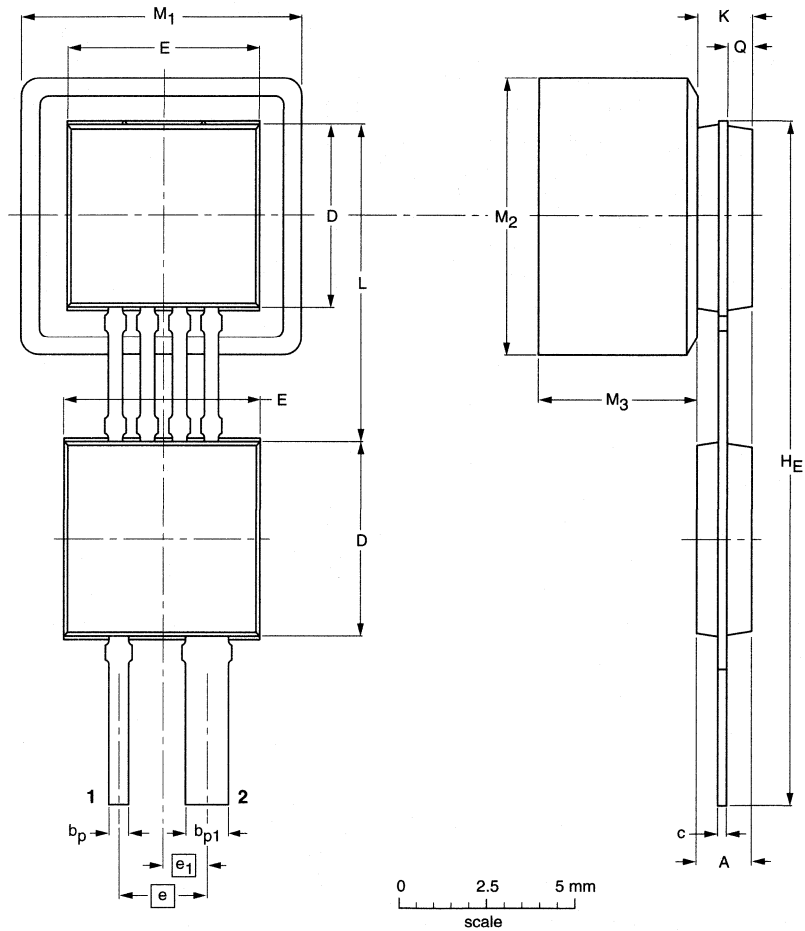
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT289A						97-06-28

Package outlines

Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8.0 x 8.0 x 4.5 mm); 2 in-line leads

SOT312A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	b <sub>p1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	H <sub>E</sub>	K <sup>(2)</sup>	L	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	Q
mm	1.67	0.6	1.3	0.31	5.7	5.7	2.5	1.25	19.0	1.70	9.1	8.2	8.2	4.7	0.8
	1.53	0.5	1.2	0.26	5.5	5.5			18.0	1.56	8.9	7.8	7.8	4.3	0.7

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. included layerthickness of glue.

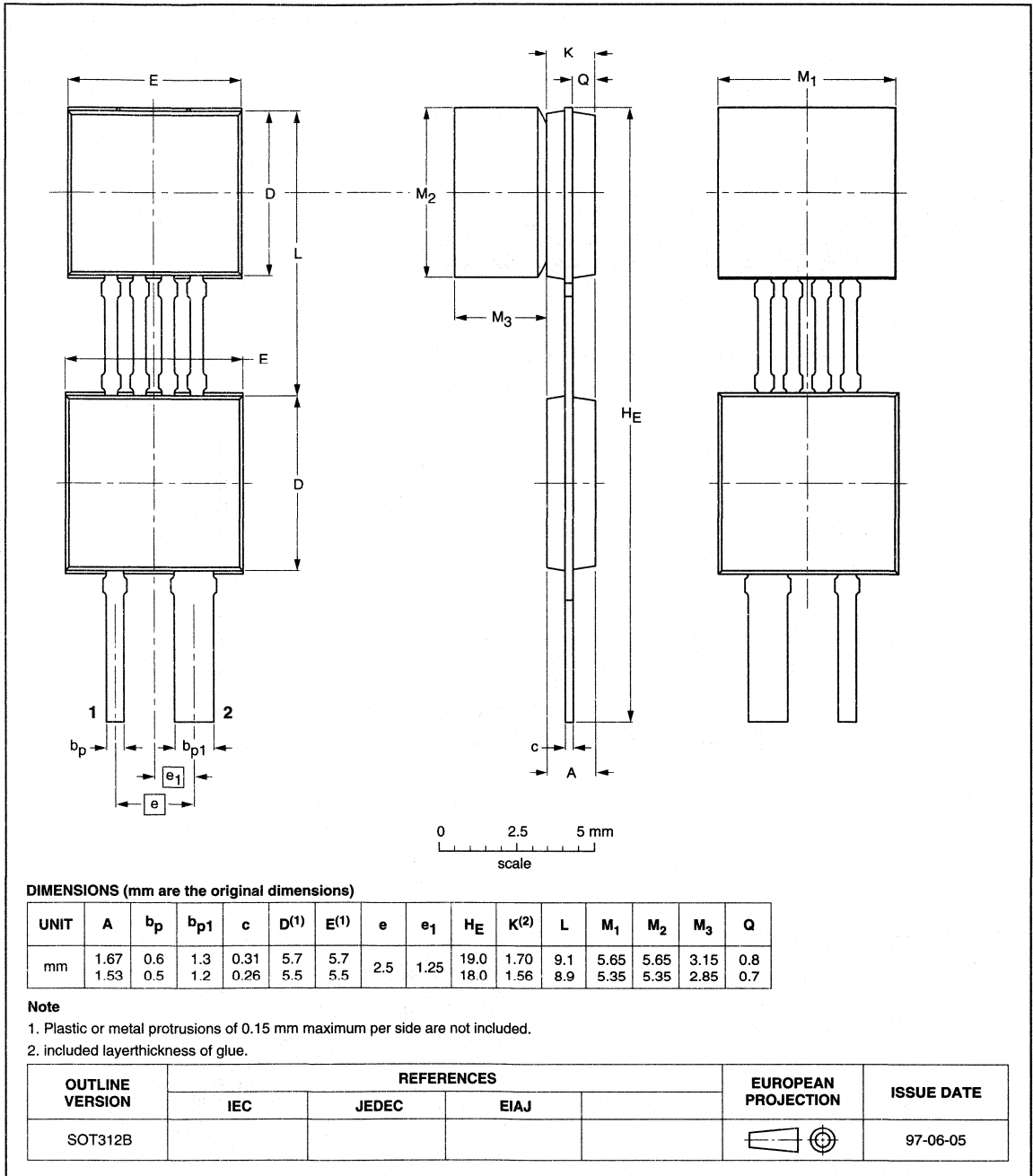
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT312A						97-06-05

Package outlines

Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 4.0 mm); 2 in-line leads

SOT312B

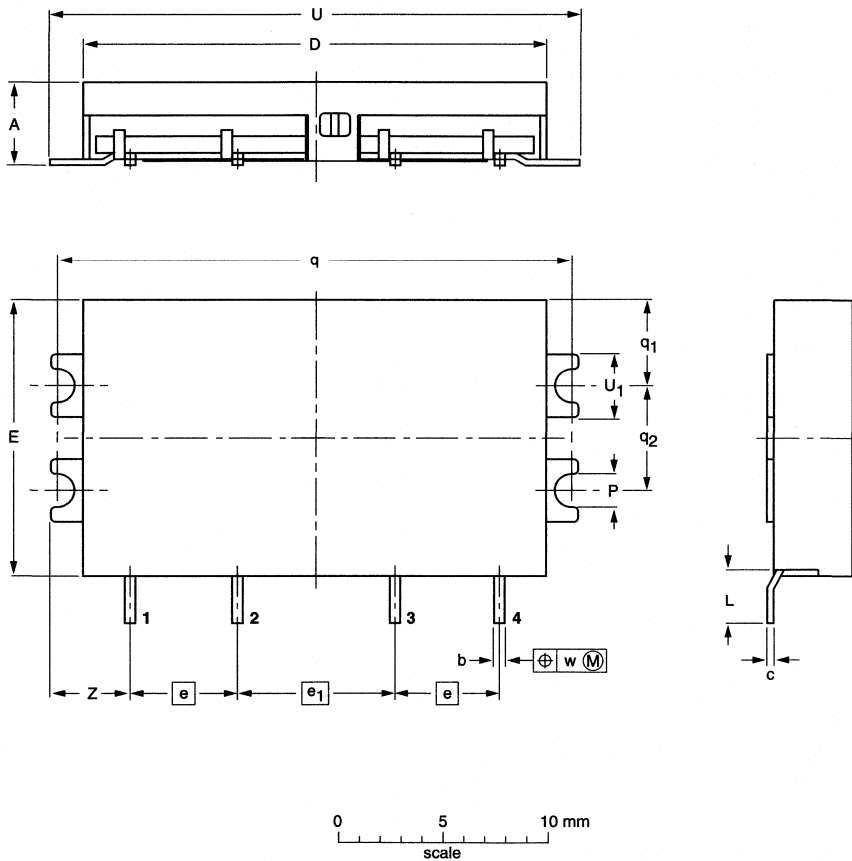


Package outlines

Chapter 2

Rectangular single-ended surface-mount package; metal cap; flange mounted; 4 in-line leads

SOT321



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	b	c	D max.	E max.	e	e <sub>1</sub>	L	P	q	q <sub>1</sub>	q <sub>2</sub>	U max.	U <sub>1</sub>	w	Z
mm	4	0.58 0.45	0.30 0.20	22.2	13.4	5.08	7.62	2.4 2.2	1.5	24.5	4.1	5	25.0	3	0.1	3.5

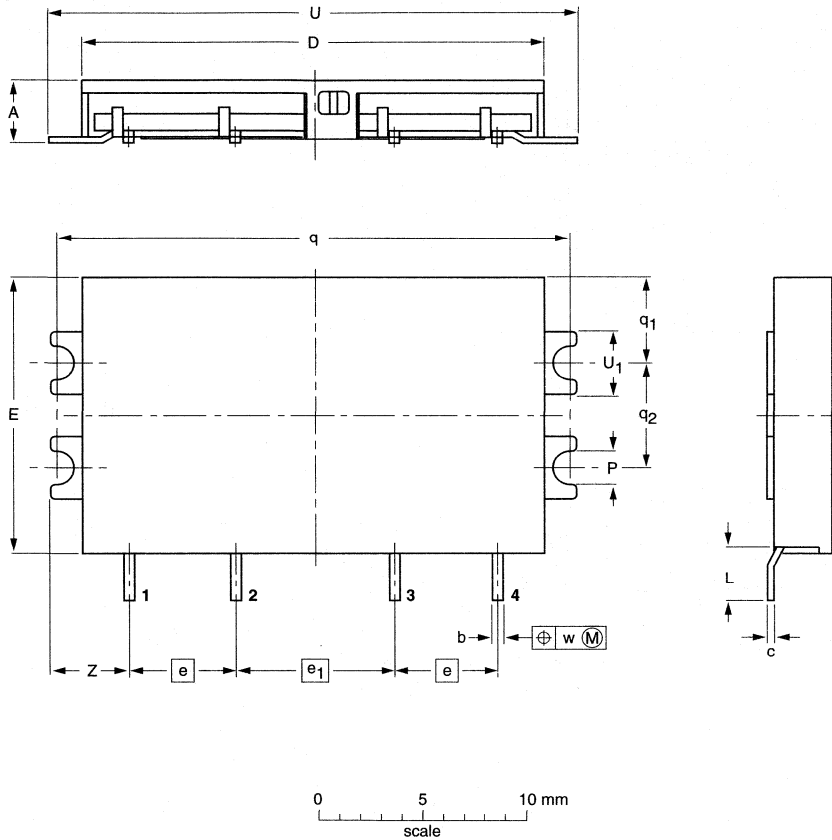
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT321					97-06-10

Package outlines

Chapter 2

Rectangular single-ended surface-mount package; metal cap; flange mounted; 4 in-line leads

SOT321B



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	b	c	D max.	E max.	e	e <sub>1</sub>	L	P	q	q <sub>1</sub>	q <sub>2</sub>	U max.	U <sub>1</sub>	w	Z
mm	3	0.58 0.45	0.30 0.20	22.2	13.4	5.08	7.62	2.4 2.2	1.5	24.5	4.1	5	25.0	3	0.1	3.5

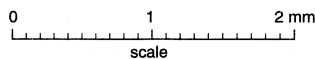
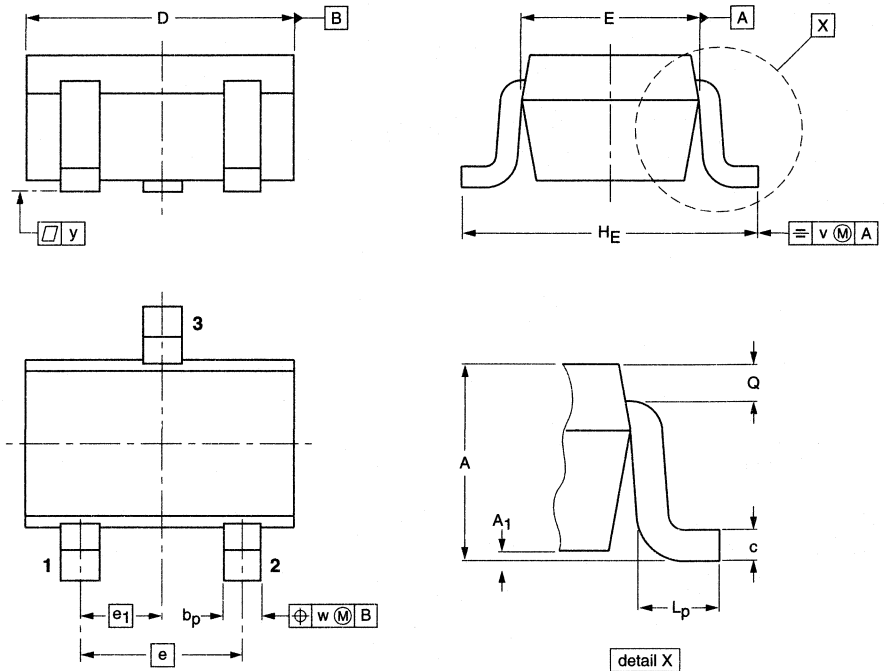
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT321B						97-04-02

Package outlines

Chapter 2

Plastic surface mounted package; 3 leads

SOT323



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

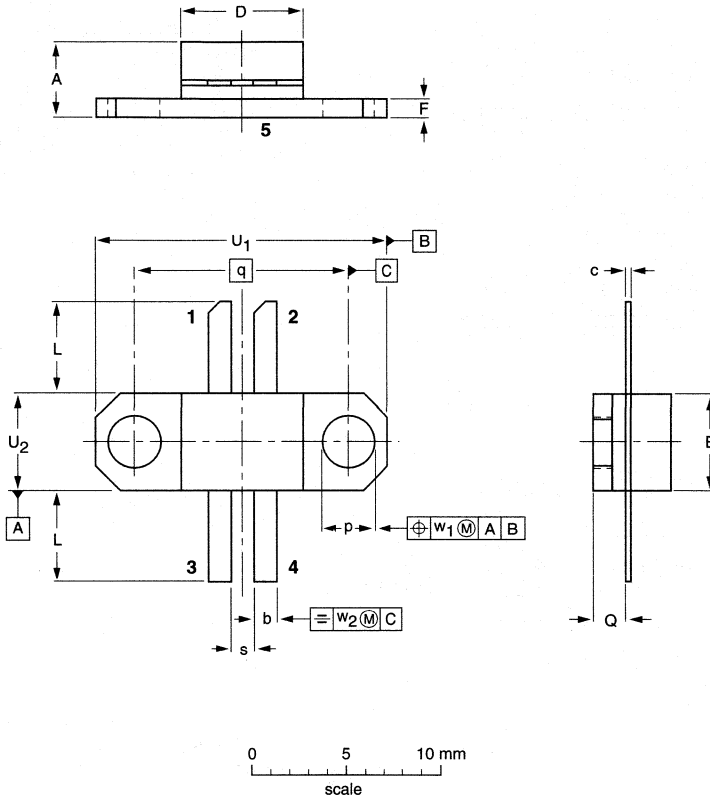


Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 4 leads

SOT324B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	L	p	Q	q	s	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.37 3.55	1.66 1.39	0.13 0.07	8.69 8.07	6.91 6.29	1.66 1.39	5.59 4.57	3.43 3.17	2.32 2.00	14.22	1.66 1.39	19.03 18.77	6.43 6.17	0.51	1.02

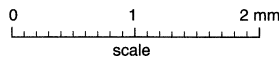
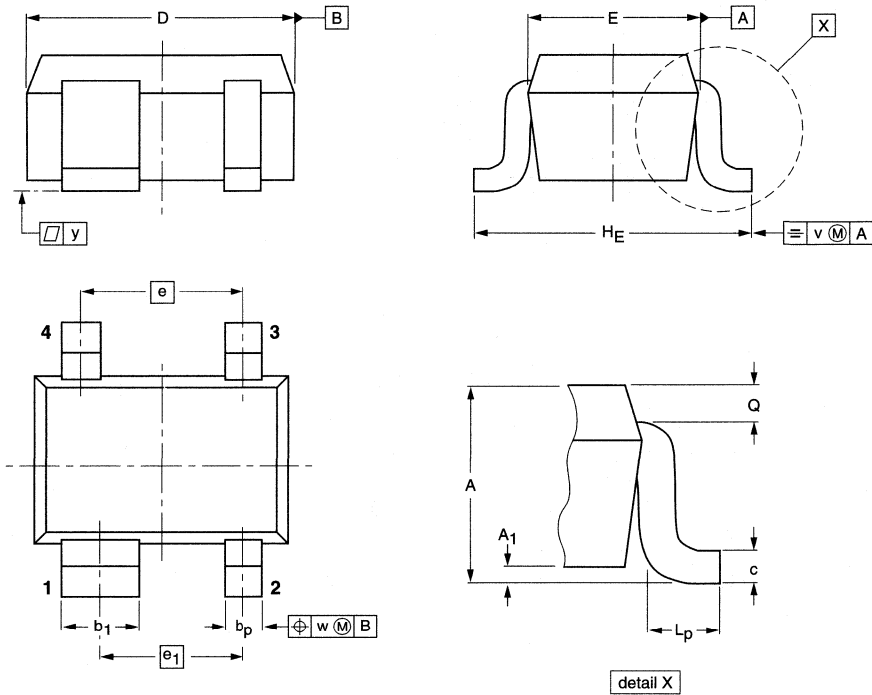
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT324B					97-06-05

Package outlines

Chapter 2

Plastic surface mounted package; 4 leads

SOT343N



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

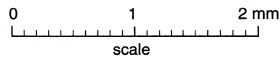
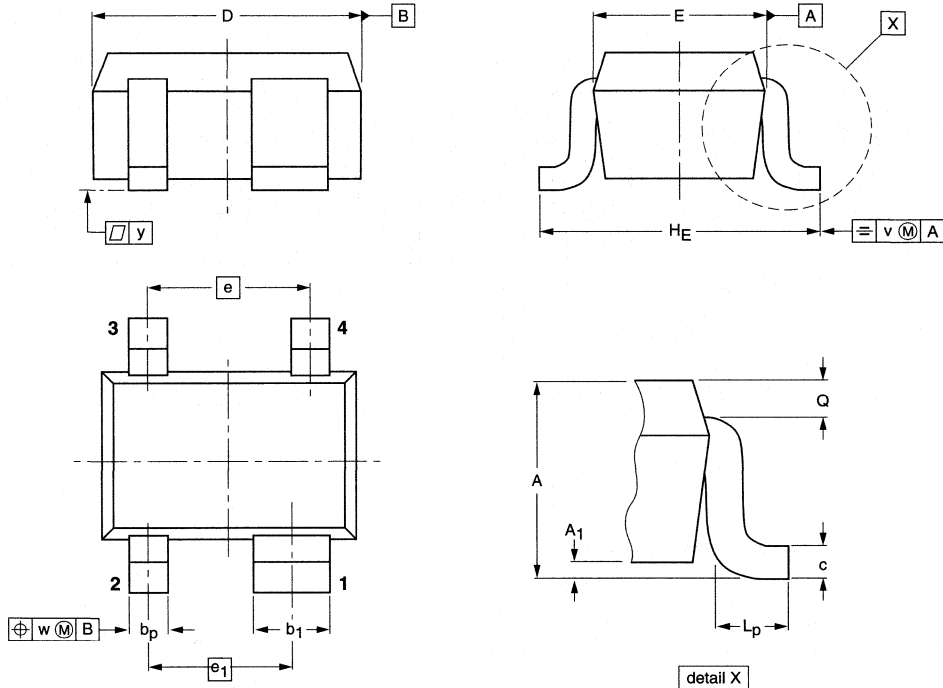
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343N						97-05-21

Package outlines

Chapter 2

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

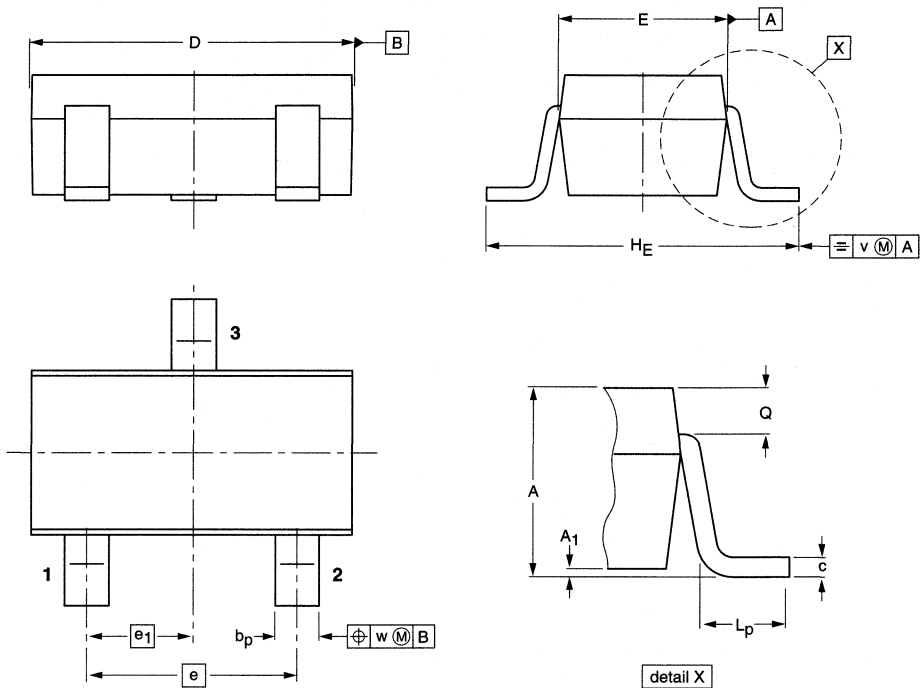
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

Package outlines

Chapter 2

Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

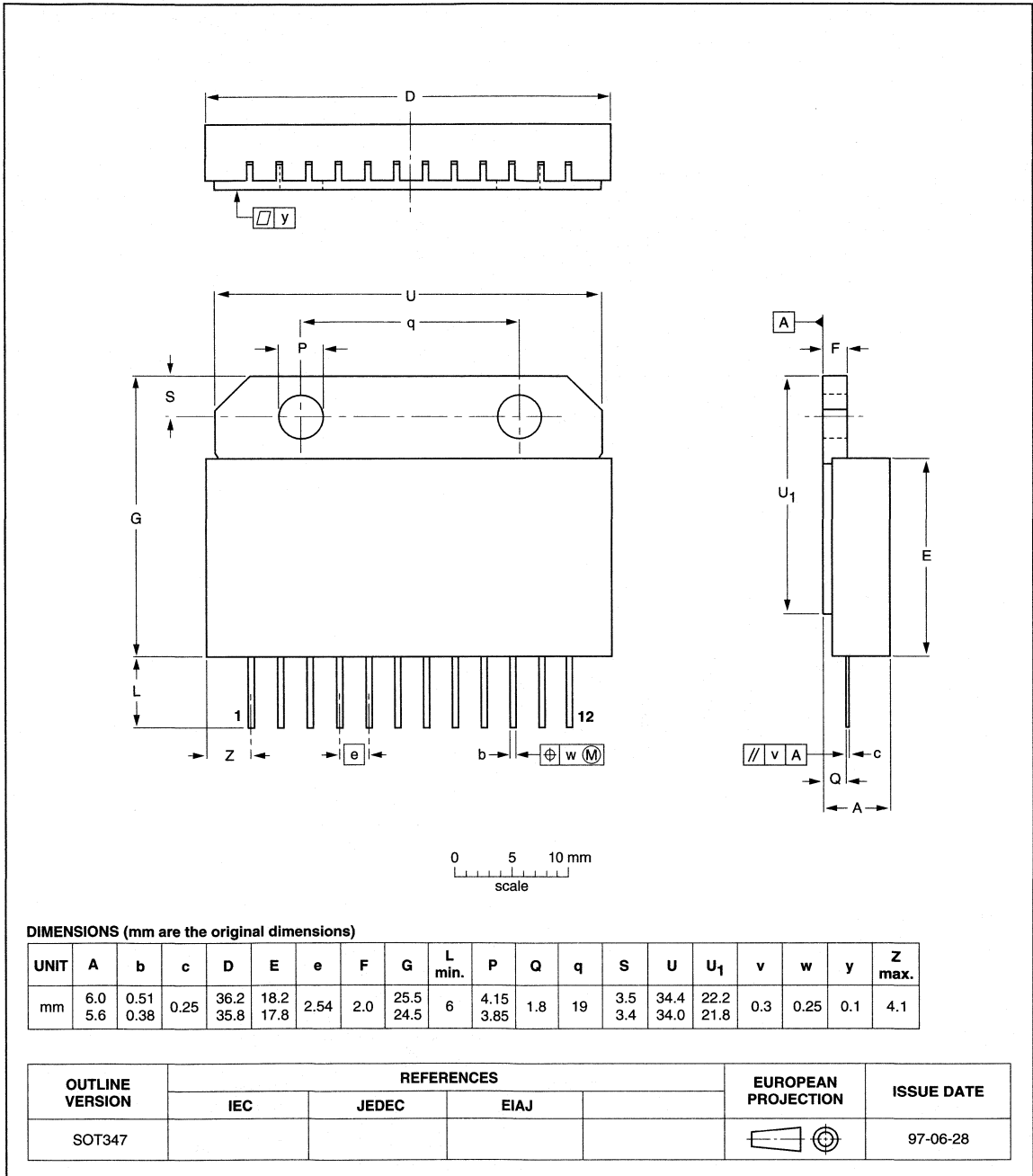
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT346		TO-236	SC-59		97-02-28

Package outlines

Chapter 2

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads

SOT347

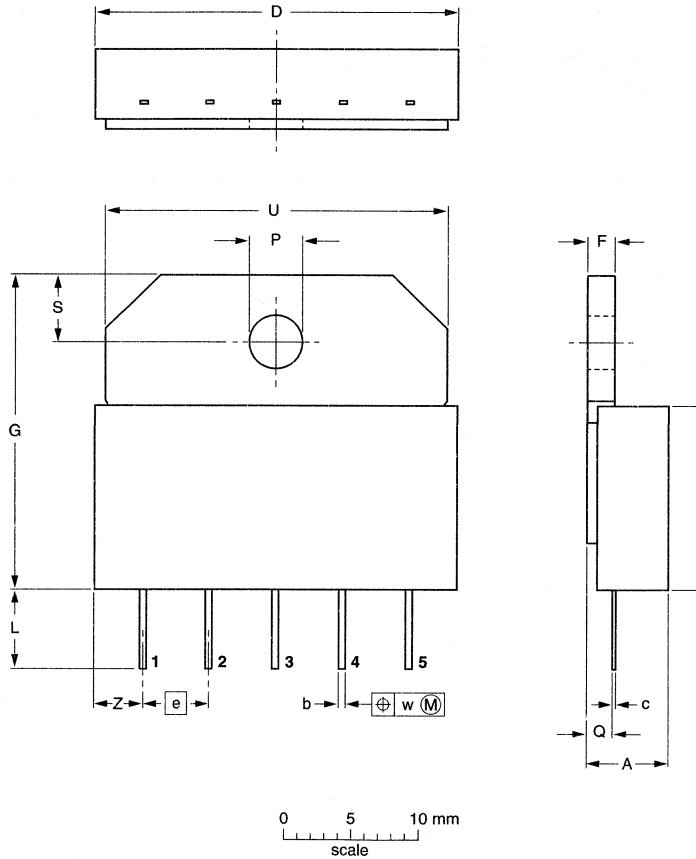


Package outlines

Chapter 2

Rectangular single-ended flat package; plastic cap; heatsink mounted; 1 mounting hole; 5 in-line gold-metallized leads

SOT348



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	b	c	D max.	E max.	e	F	G max.	L min.	P	Q	S	U	w	Z max.
mm	6.0	0.51 0.38	0.25	27.2	13.8	5.08	2.0	23.5	6	4.15 3.85	1.8	5	25.5	0.25	3.8

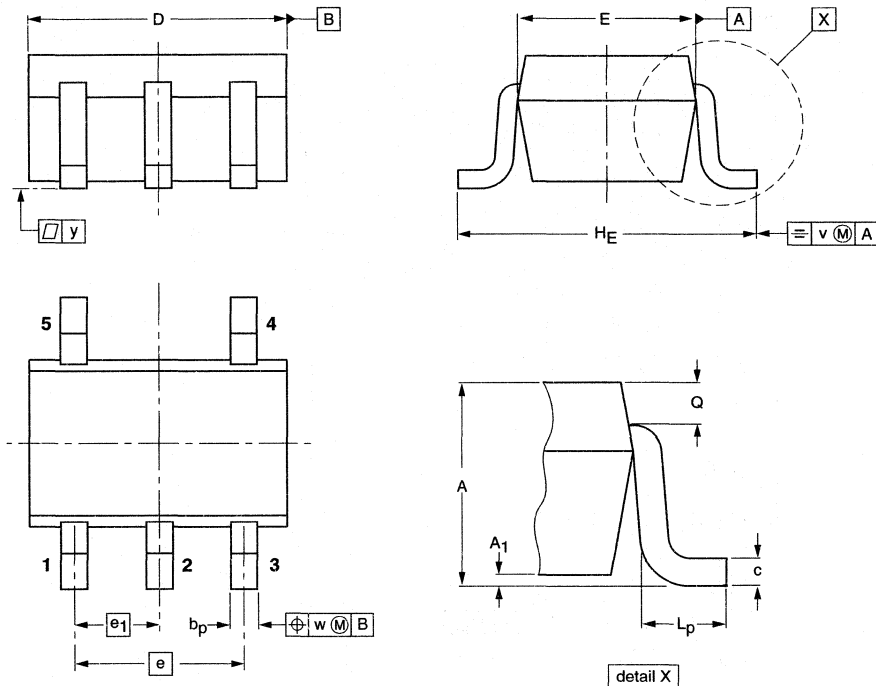
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT348					97-04-14

Package outlines

Chapter 2

Plastic surface mounted package; 5 leads

SOT353



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E <sup>(2)</sup>	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

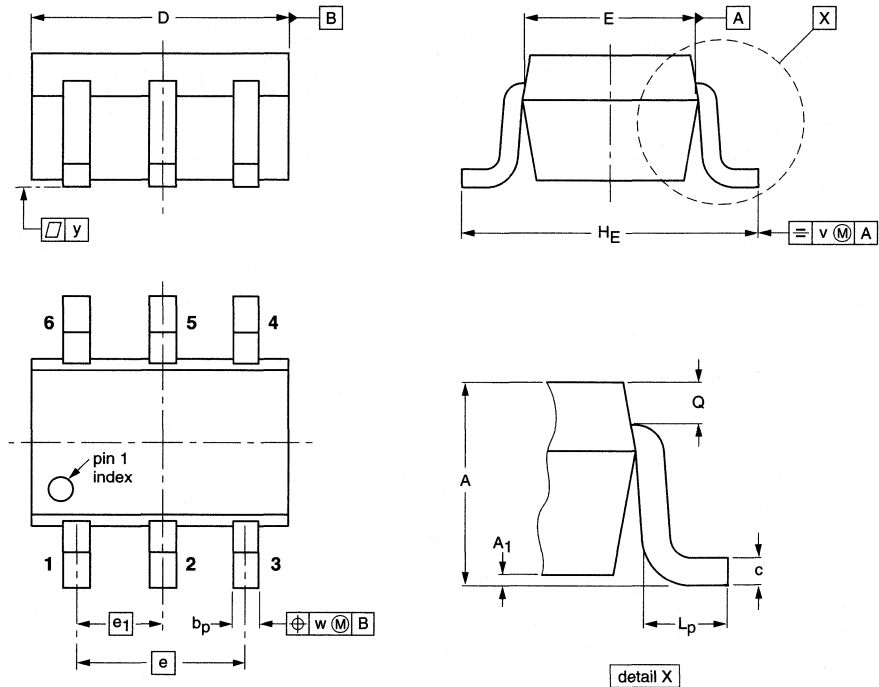
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT353			SC-88A		97-02-28

Package outlines

Chapter 2

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A1 max	bp	c	D	E	e	e1	HE	Lp	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

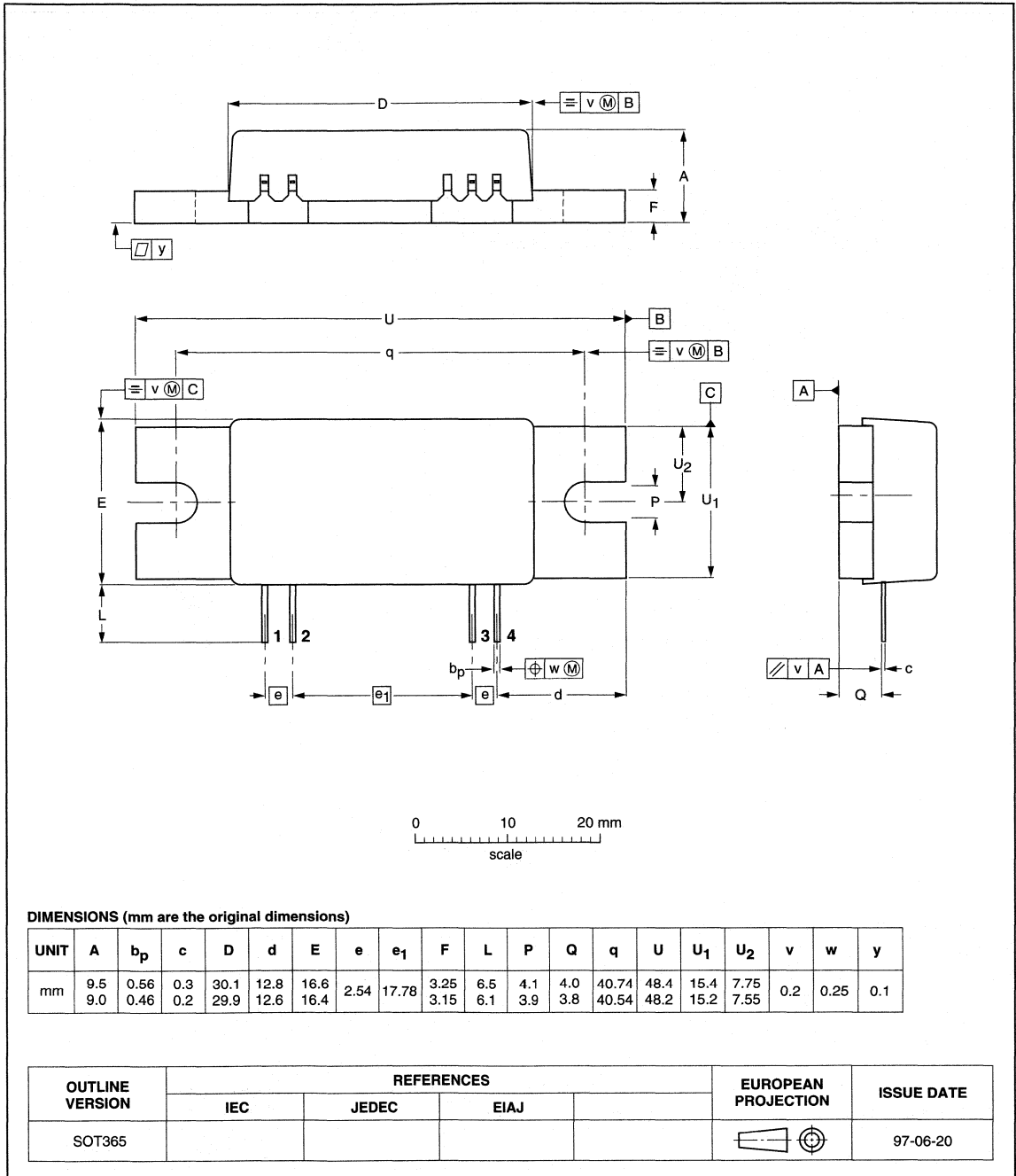
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28



Package outlines

Chapter 2

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads SOT365

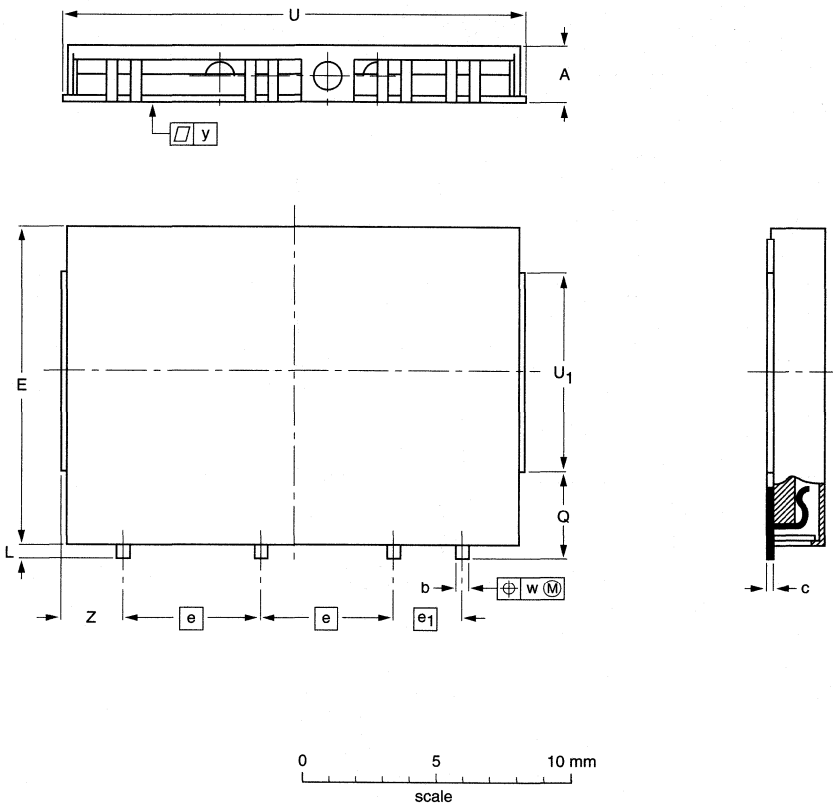


Package outlines

Chapter 2

Rectangular single-ended surface-mount package; metal cap; 4 in-line leads

SOT388A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	e	e <sub>1</sub>	E	L	Q	U	U <sub>1</sub>	w	y	Z
mm	2.2 1.8	0.56 0.46	0.30 0.20	5.08	2.54	12.2 11.8	0.7 0.3	3.45 3.05	17.3 16.9	7.7 7.3	0.25	0.15	2.3 1.9

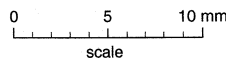
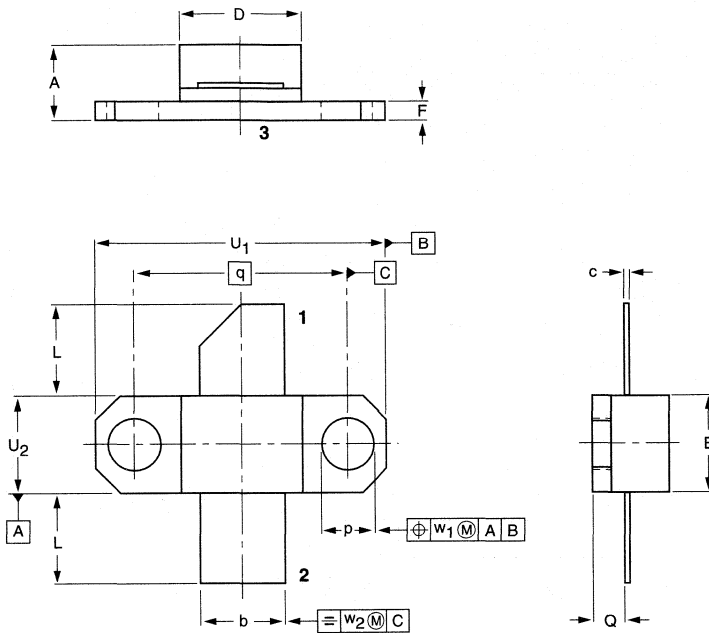
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT388A					97-04-18

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 2 leads

SOT390A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.37 3.55	5.72 5.46	0.16 0.10	8.69 8.07	6.91 6.29	1.66 1.39	6.10 5.33	3.43 3.17	2.32 2.00	14.22	19.03 18.77	6.43 6.17	0.51	1.02

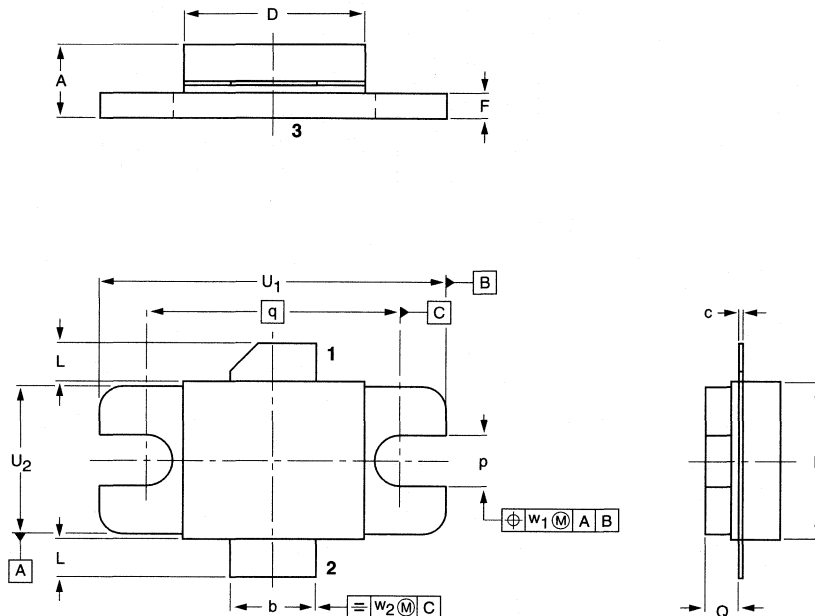
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT390A						97-05-29

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 2 leads

SOT391A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	L	p	Q	q	$U_1$	$U_2$	$w_1$	$w_2$
mm	5.36	5.85	0.16	11.54	10.93	1.66	2.79	3.43	2.29	16.51	22.99	9.91	0.51	1.02
	4.29	5.58	0.10	10.51	9.90	1.39	2.29	3.17	2.03	16.51	22.73	9.65	0.51	1.02

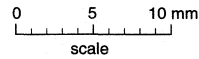
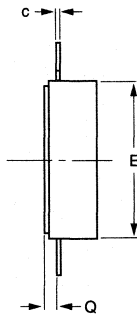
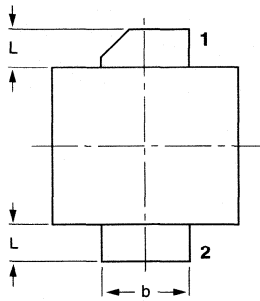
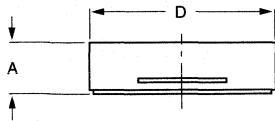
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT391A					97-05-29

Package outlines

Chapter 2


Flangeless ceramic package; 2 leads

SOT391B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

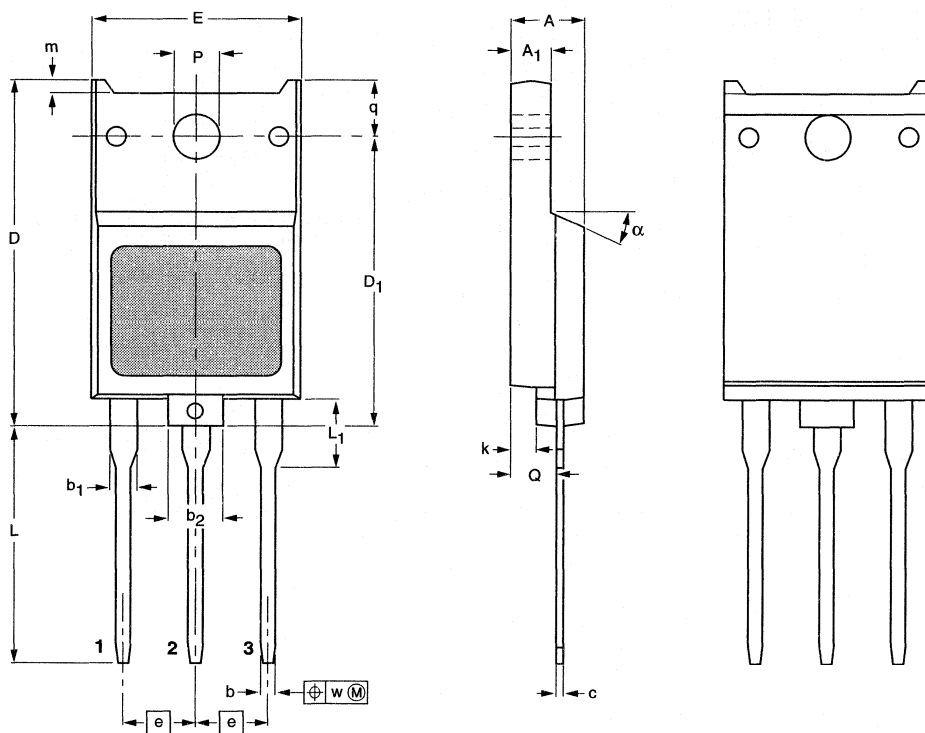
UNIT	A	b	c	D	E	L	Q
mm	4.09 3.02	5.85 5.58	0.16 0.10	11.54 10.51	10.93 9.90	2.79 2.29	1.02 0.76

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391B						97-05-29

Package outlines

Chapter 2

Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads SOT399



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	k	L	L <sub>1</sub> <sup>(1)</sup>	m	P	Q	q	w	α
mm	5.8	3.3	1.2	2.2	4.7	0.9	27	22.5	16	5.45	2.2	19.1	5.4	0.8	3.4	3.4	4.7	0.4	27°
	4.8	2.7	0.9	1.8	4.2	0.6	26	21.5	15		1.8	18.1	4.8	0.6	3.1	3.2	4.3		23°

**Note**

1. Tinning of terminals uncontrolled in this zone.
2. All release angles 5°

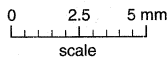
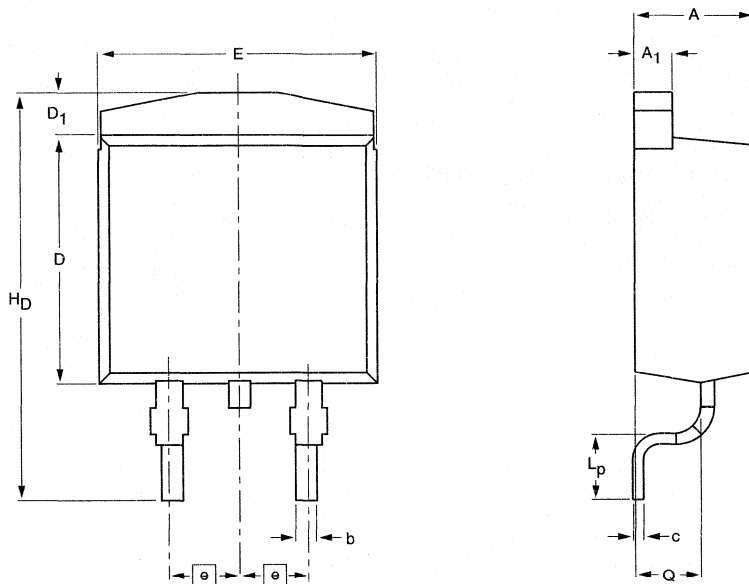
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT399						97-06-11

Package outlines

Chapter 2

Plastic single-ended package (Philips version of D2-PAK); 2 leads

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.5	1.40	0.85	0.64	9.65	1.6	10.3	2.54	2.9	15.4	2.60
	4.1	1.27	0.60	0.46	8.65	1.2	9.7		2.1	14.8	2.20

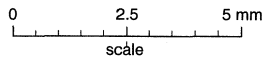
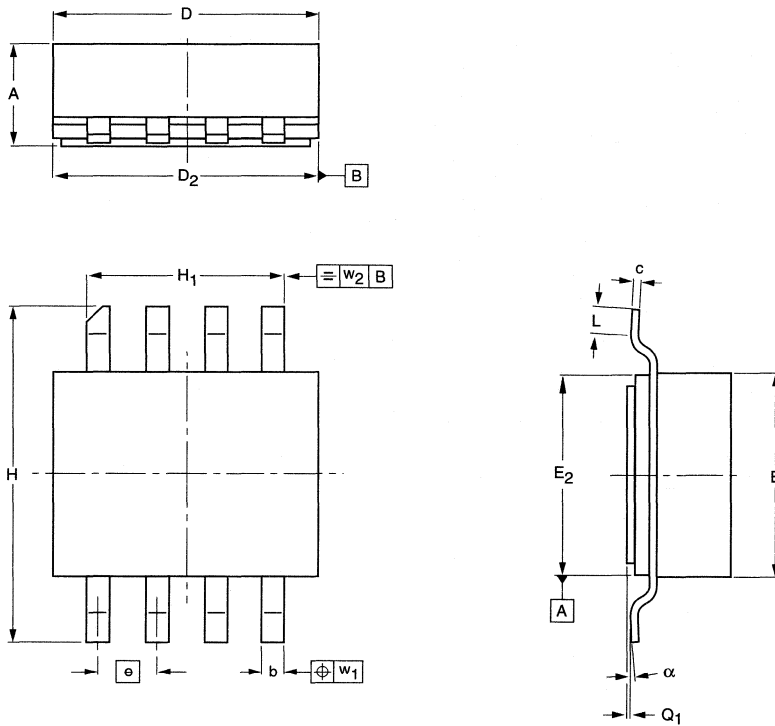
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT404					97-06-16

Package outlines

Chapter 2

Ceramic surface mounted package; 8 leads

SOT409A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>2</sub>	E	E <sub>2</sub>	e	H	H <sub>1</sub>	L	Q <sub>1</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						97-06-28

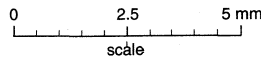
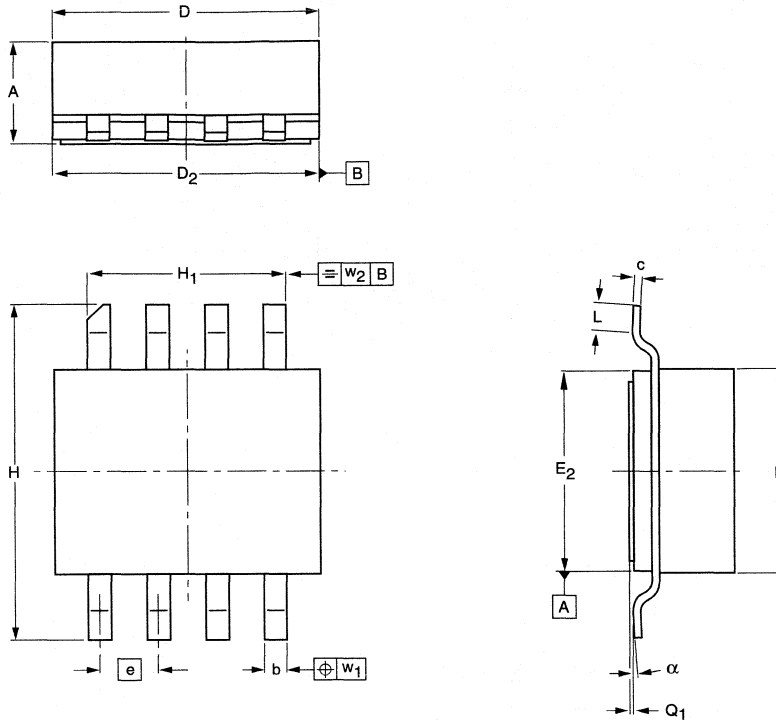


Package outlines

Chapter 2

Ceramic surface mounted package; 8 leads

SOT409B



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D <sub>2</sub>	E	E <sub>2</sub>	e	H	H <sub>1</sub>	L	Q <sub>1</sub>	w <sub>1</sub>	w <sub>2</sub>	α
mm	2.36 2.06	0.58 0.43	0.15 0.10	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	0.84 0.69	0.10 0.00	0.25	0.25	2° 0°
inches	0.093 0.081	0.023 0.017	0.006 0.004	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.033 0.027	0.004 0.000	0.010	0.010	2° 0°

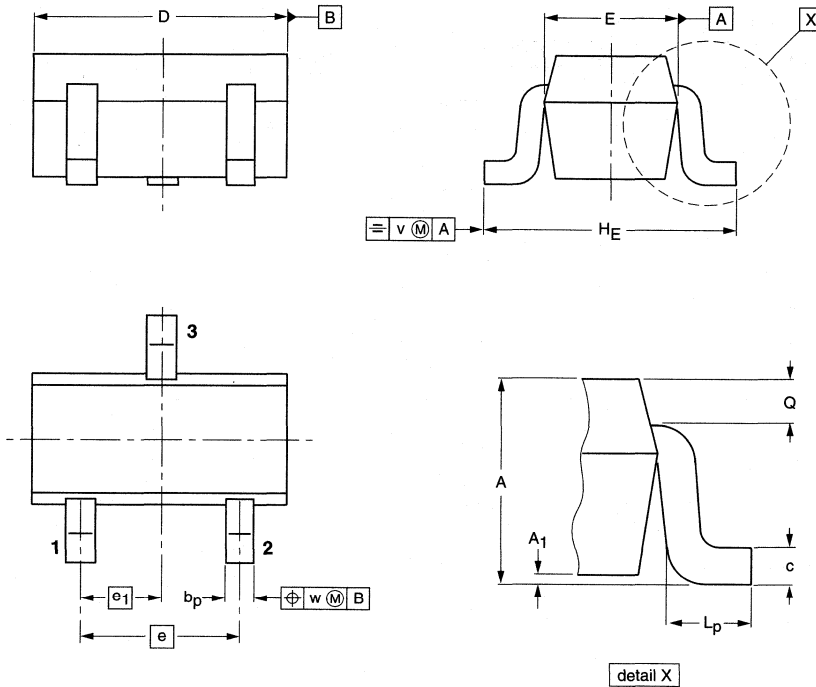
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409B						97-06-28

Package outlines

Chapter 2

Plastic surface mounted package; 3 leads

SOT416



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

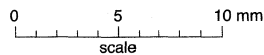
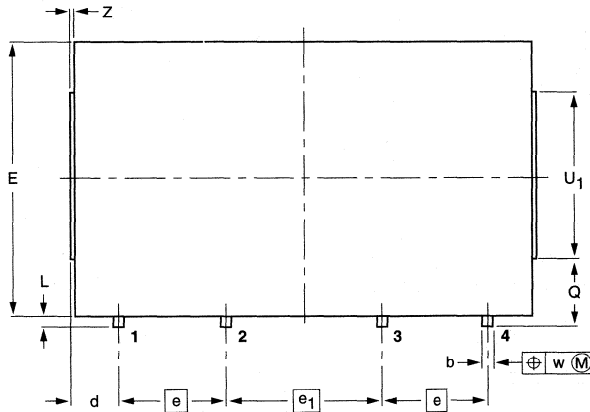
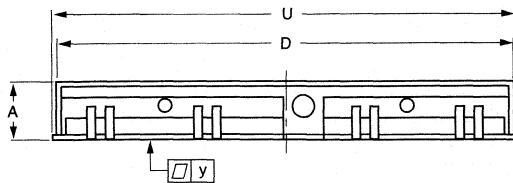
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

Package outlines

Chapter 2

Ceramic single-ended flat package; 4 in-line leads

SOT421A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	d	E	e	e <sub>1</sub>	L	Q	U	U <sub>1</sub>	w	y	Z
mm	3.0 2.6	0.56 0.46	0.30 0.20	22.1 21.7	2.4 2.0	13.4 13.0	5.08	7.62	0.7 0.3	3.4 3.0	22.4 22.0	8.2 7.8	0.25	0.15	0.25 0.05

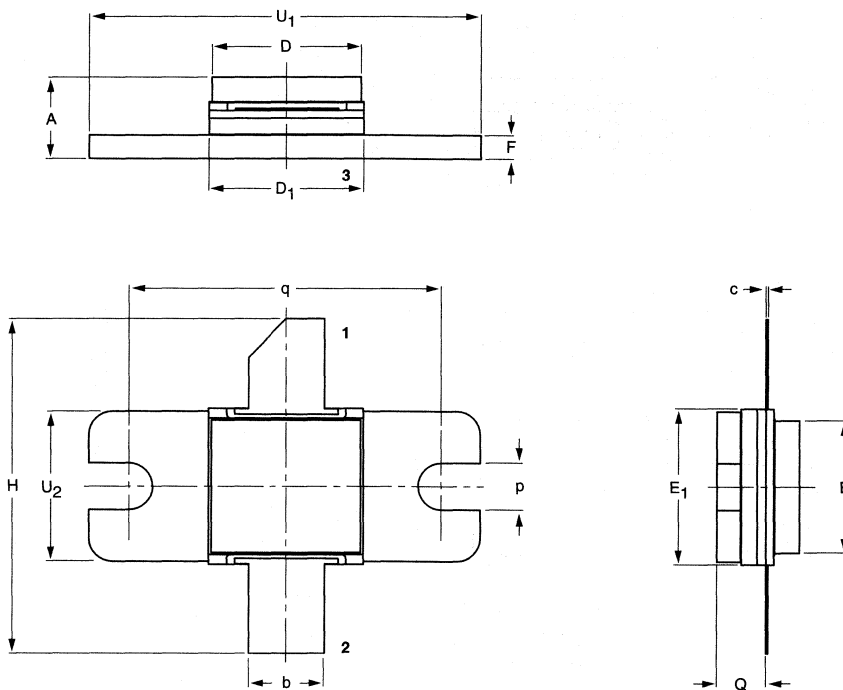
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT421A						97-06-20

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT422A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>
mm	5.58	5.21	0.16	9.93	10.29	8.77	10.29	1.58	21.97	3.43	3.34	16.64	22.99	9.91
	5.04	4.95	0.10	9.67	10.03	8.51	10.03	1.46	21.71	3.17	2.96	16.38	22.73	9.65

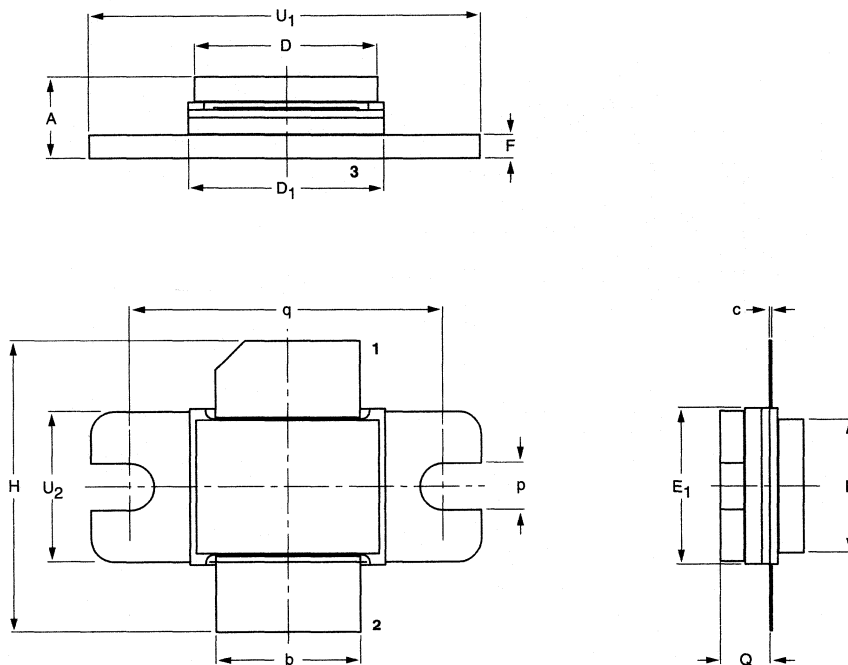
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT422A						97-04-01

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT423A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>
mm	5.58 5.04	9.53 9.27	0.16 0.10	12.02 11.76	12.83 12.57	8.82 8.56	10.29 10.03	1.58 1.46	19.18 18.92	3.43 3.17	3.42 2.88	16.64 16.38	22.99 22.73	9.91 9.65

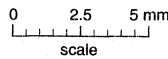
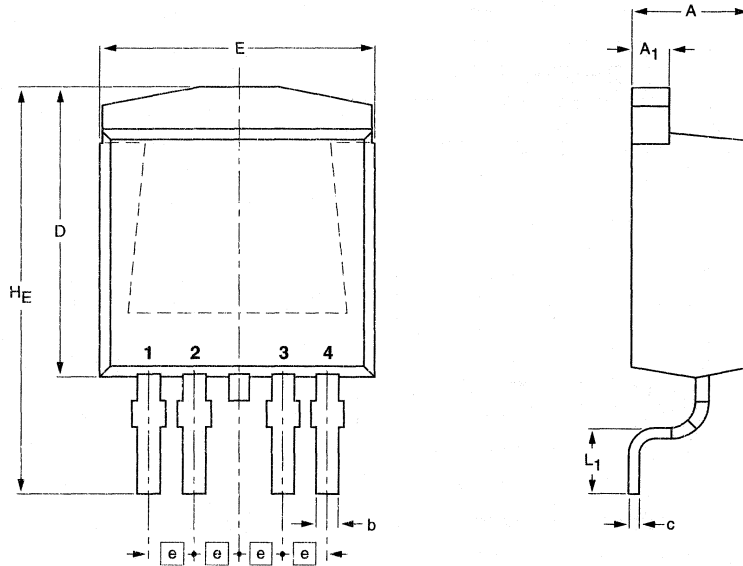
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT423A						97-04-01

Package outlines

Chapter 2

Plastic single-ended package (Philips version of D2-PAK); 4 leads

SOT426



DIMENSIONS (mm are the original dimensions) \*

UNIT	A	A <sub>1</sub>	b	c	D max.	E	e	L <sub>1</sub>	H <sub>E</sub>
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	10.30 9.70	1.70	2.90 2.10	15.80 14.80

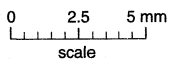
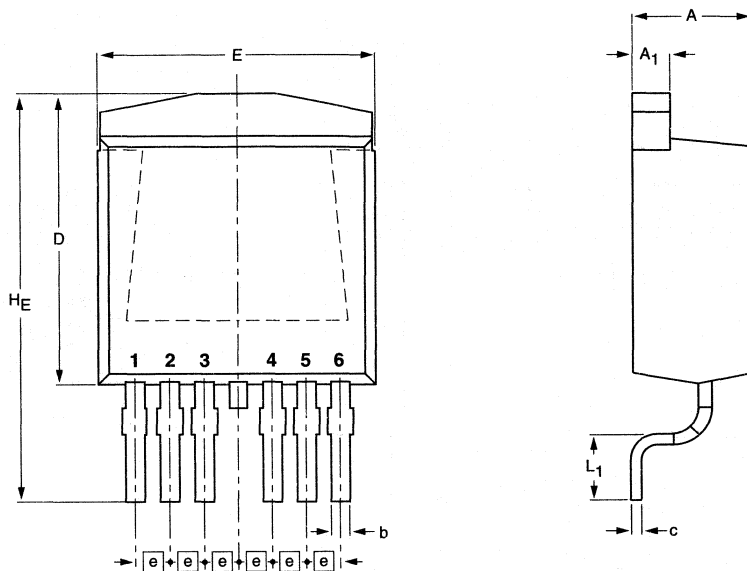
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT426						97-06-11

Package outlines

Chapter 2

Plastic single-ended package (Philips version of D2-PAK); 6 leads

SOT427



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	E	e	L <sub>1</sub>	H <sub>E</sub>
mm	4.50 4.10	1.40 1.27	0.7 0.4	0.64 0.46	11	10.30 9.70	1.27	2.90 2.10	15.80 14.80

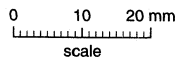
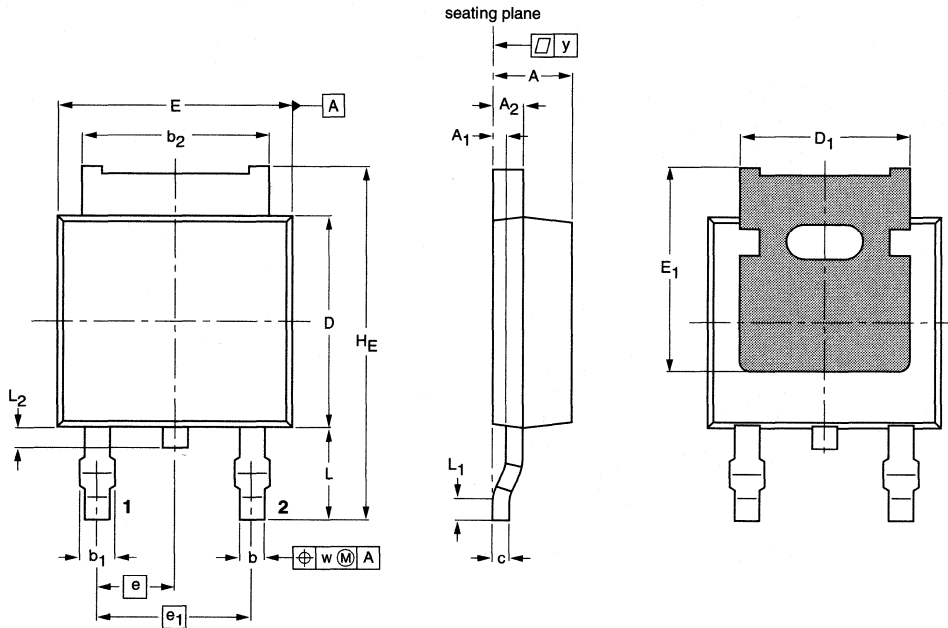
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT427						97-06-11

Package outlines

Chapter 2

Plastic surface mounted package (Philips version of D-PAK); 2 leads

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> (1)	A <sub>2</sub>	b	b <sub>1</sub> max.	b <sub>2</sub>	c	D max.	D <sub>1</sub> max.	E max.	E <sub>1</sub> min.	e	e <sub>1</sub>	H <sub>E</sub> max.	L	L <sub>1</sub> min.	L <sub>2</sub>	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						97-06-11

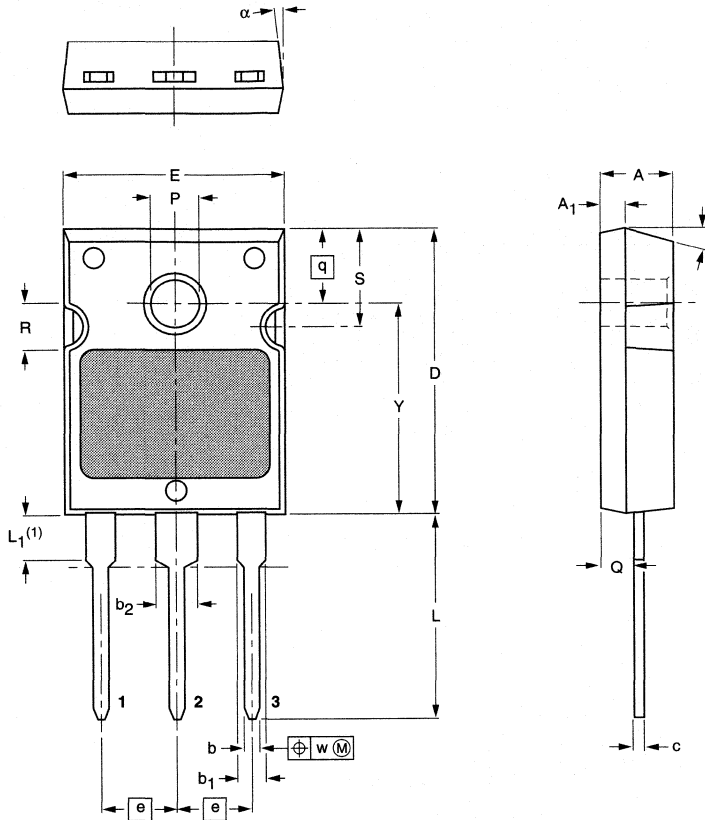


Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-247

SOT429



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	E	e	L	L <sub>1</sub>	P	Q	q	R	S	w	Y	α	β
mm	5.3	1.9	1.2	2.2	3.2	0.9	21	16	5.45	16	4.0	3.7	2.6	5.3	3.5	7.5	0.4	15.7	6°	17°
	4.7	1.7	0.9	1.8	2.8	0.6	20	15		15	3.6	3.3	2.4		3.3	7.1		15.3	4°	13°

Note

1. Terminals are uncontrolled within zone L<sub>1</sub>.

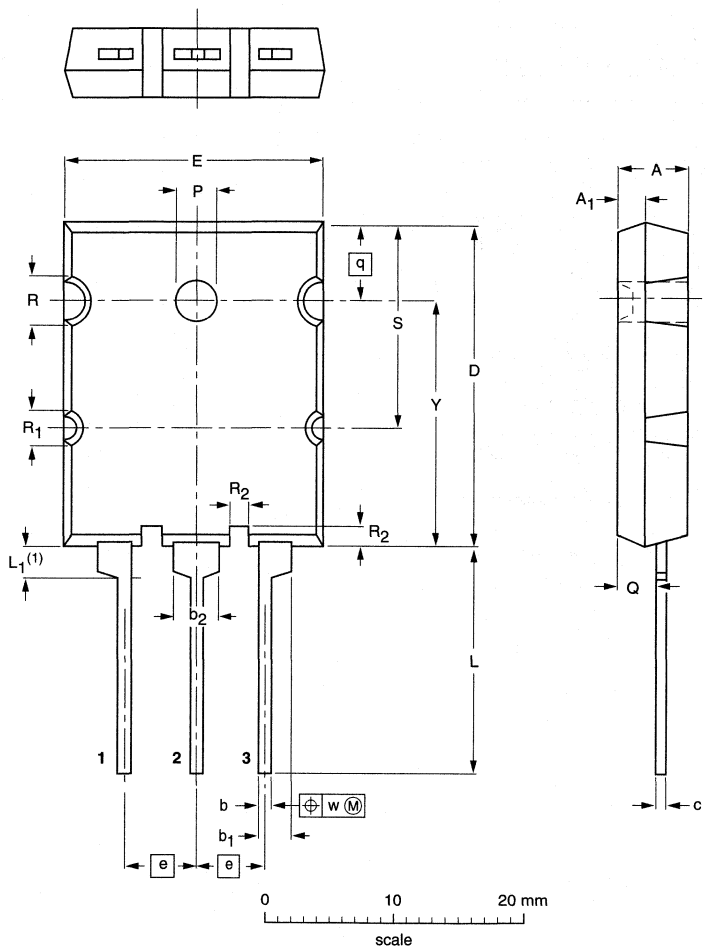
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT429		TO-247				97-06-11

Package outlines

Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead JUMBO TO-247

SOT430



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	b	b <sub>1</sub> max.	b <sub>2</sub> max.	c max.	D	E max.	e	L min.	L <sub>1</sub>	P	Q max.	q	R	R <sub>1</sub>	R <sub>2</sub>	S	w	Y
mm	5.3	2.3	1.0 0.8	2.5	3.5	0.8	26.5 25.5	20.5	5.45	19.5	2.5	3.5 3.1	3.0	6.0	4.0	3.0	1.5	16	0.4	20.5 19.5

Note

1. Terminals are uncontrolled within zone L<sub>1</sub>.

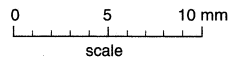
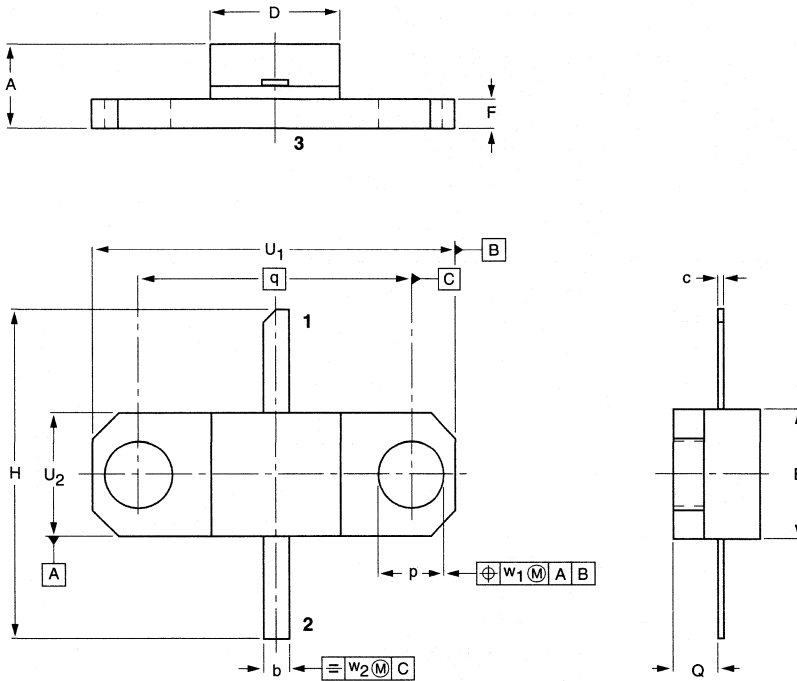
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT430						97-06-23

Package outlines

Chapter 2

Flanged ceramic package; 2 mounting holes; 2 leads

SOT437A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	5.03 4.31	1.66 1.39	0.13 0.07	6.99 6.22	6.99 6.22	1.66 1.39	17.02 16.00	3.43 3.17	2.29 2.03	14.22	19.03 18.77	6.48 6.22	0.51	1.02

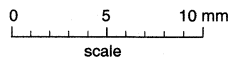
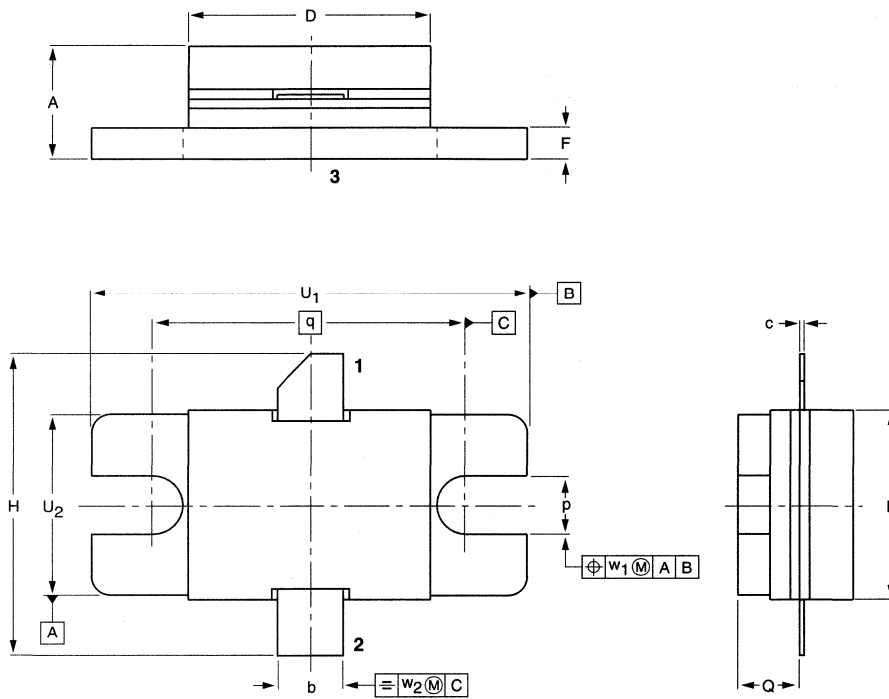
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT437A					97-05-23

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT439A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	6.05 5.13	3.69 3.42	0.13 0.05	13.09 12.57	10.55 10.03	1.58 1.47	17.28 15.74	3.43 3.17	3.36 2.92	16.51	22.94 22.73	9.91 9.65	0.51	1.02

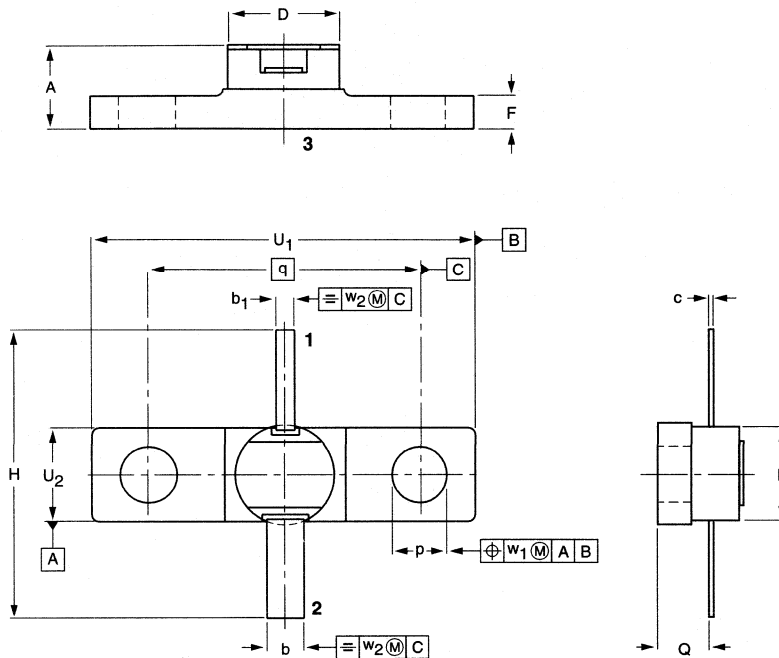
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT439A					97-05-23

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT440A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	E	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.25 3.27	2.16 1.90	1.15 0.88	0.16 0.07	5.85 5.58	5.31 5.00	1.66 1.39	15.75 14.73	3.18 2.92	3.48 2.92	14.22	20.45 20.19	5.21 4.95	0.51	1.02

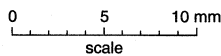
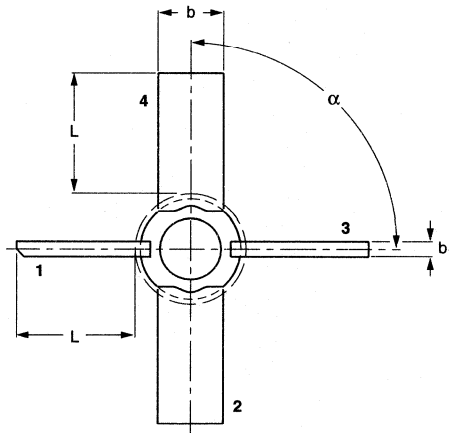
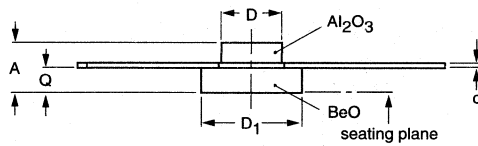
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT440A					97-05-23

Package outlines

Chapter 2

Studless ceramic package; 4 leads

SOT441A



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	b	b <sub>1</sub>	c	D	D <sub>1</sub>	L min.	Q	$\alpha$
mm	2.4	3.2	0.75	0.125	3.38 3.08	5.28 5.12	6	1.3 1.0	90°

Note

1. This device incorporates naked beryllium oxide, the dust of which is toxic.

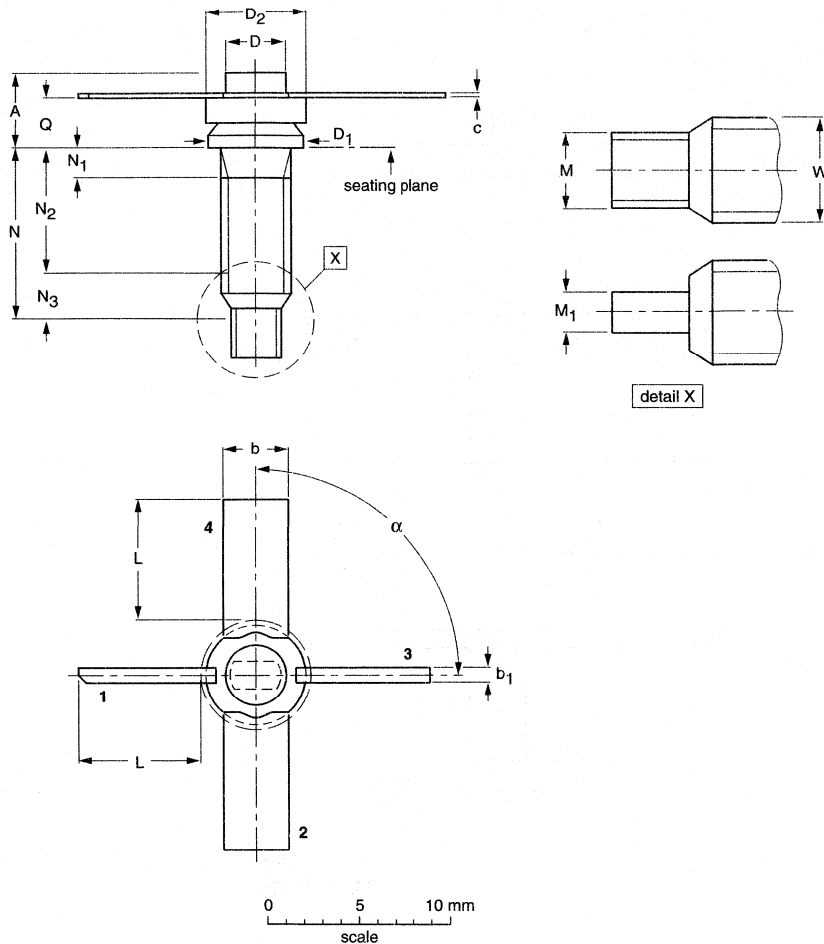
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT441A					97-02-28

Package outlines

Chapter 2

Studded ceramic package; 4 leads

SOT442A



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	b	b <sub>1</sub>	c	D	D <sub>1</sub>	D <sub>2</sub>	L min.	M	M <sub>1</sub>	N max.	N <sub>1</sub> max.	N <sub>2</sub>	N <sub>3</sub> min	Q	W	$\alpha$
mm	4.0	3.2	0.75	0.125	3.38 3.08	5.25 5.10	5.28 5.12	6	3.27 3.01	1.6 1.4	12.5	1.6	8.5 7.5	2.9	2.80 2.50	8-32 UNC	90°

Note

1. This device incorporates naked beryllium oxide, the dust of which is toxic.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT442A					97-02-28



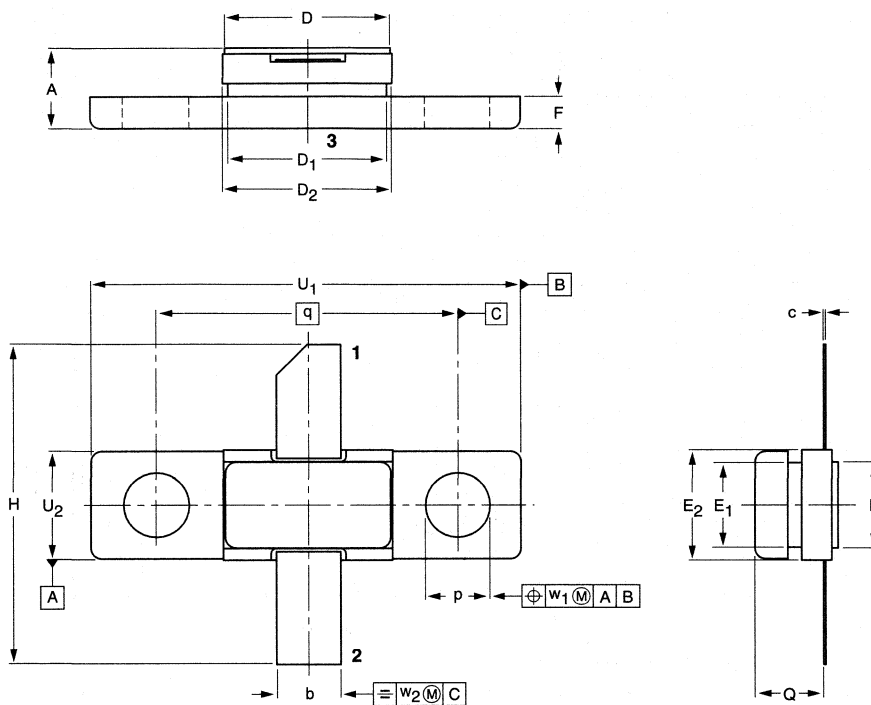


Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT445A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.01 3.36	3.15 2.95	0.15 0.09	7.9 7.7	7.65 7.35	8.15 7.85	4.1 3.9	4.25 3.95	5.31 5.01	1.82 1.22	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.51	1.02

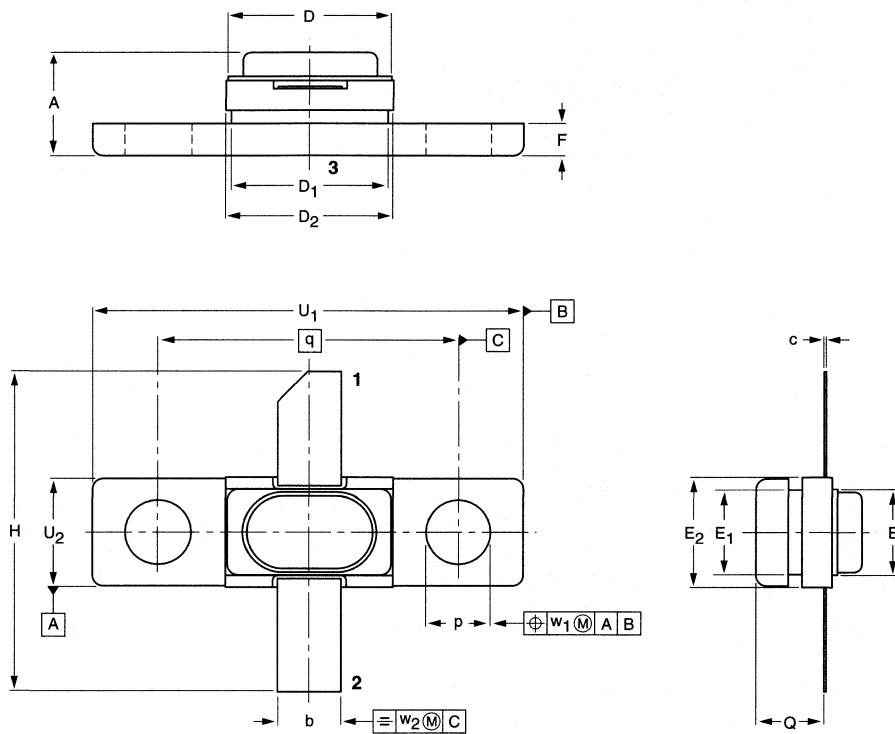
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445A						97-05-26

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT445B



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	5.27 4.50	3.15 2.95	0.15 0.09	7.85 7.74	7.65 7.35	8.15 7.85	3.97 3.86	4.25 3.95	5.31 5.01	1.82 1.22	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.51	1.02

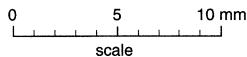
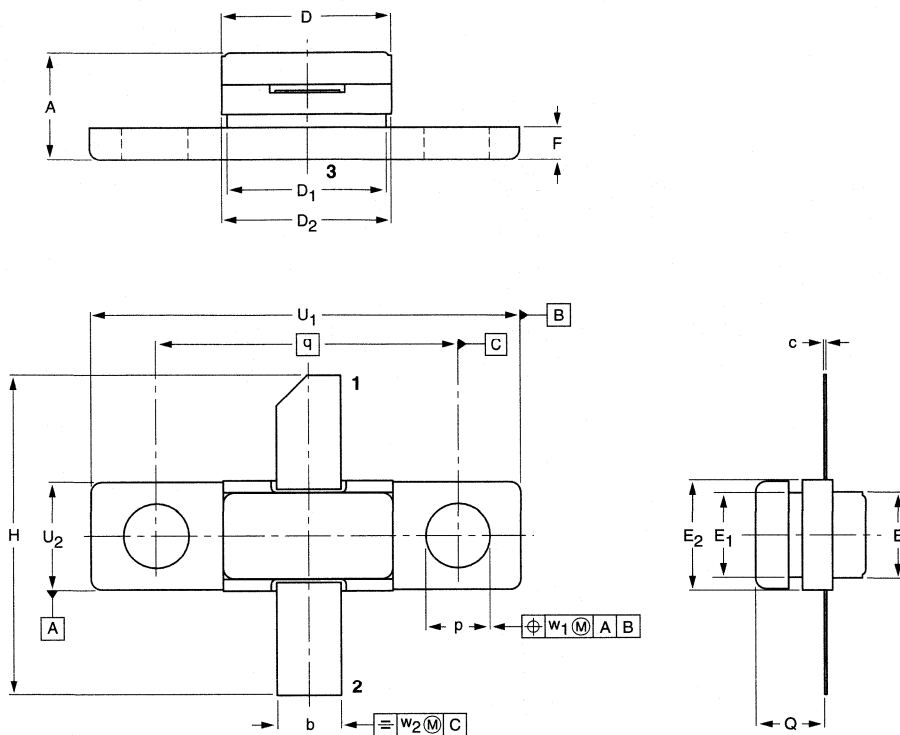
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT445B					97-05-27

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT445C



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	E <sub>2</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	5.57 4.70	3.15 2.95	0.15 0.09	8.13 7.87	7.65 7.35	8.15 7.85	4.20 3.93	4.25 3.95	5.31 5.01	1.82 1.22	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.51	1.02

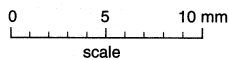
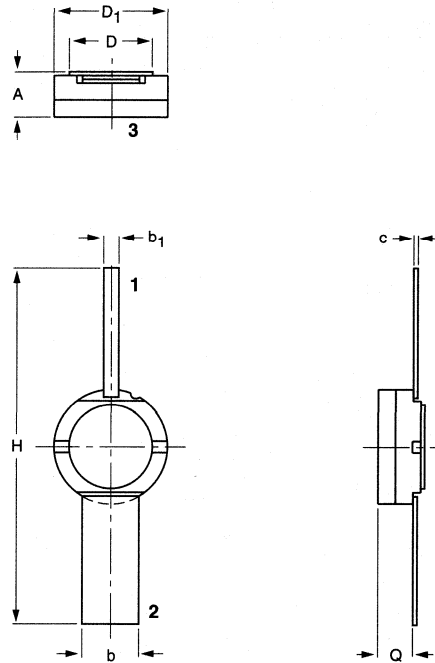
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445C						97-05-23

Package outlines

Chapter 2

Studless hermetic ceramic package; 2 leads

SOT446A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b <sub>1</sub>	c	D	D <sub>1</sub>	H	Q
mm	2.67	3.08	0.92	0.16	4.42	6.00	19.56	2.24
	1.99	2.76	0.60	0.07	4.21	5.68	17.52	1.62

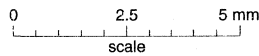
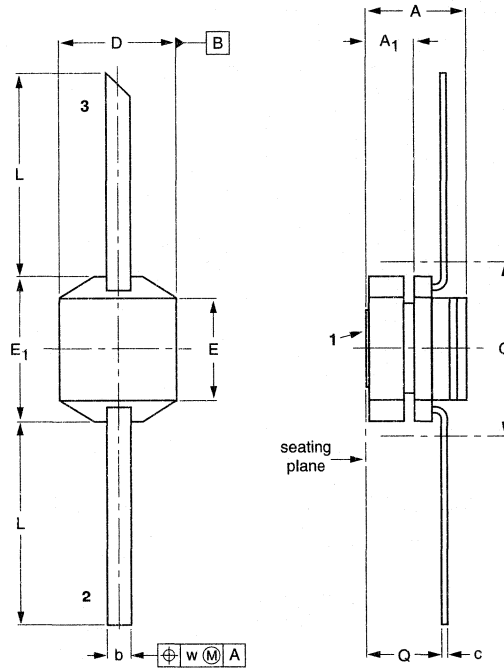
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT446A					97-05-23

Package outlines

Chapter 2

Flangeless ceramic package; 2 leads

SOT447A



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> max.	b	c	D	E	E <sub>1</sub>	G max.	L min.	Q	w
mm	2.8	1.3	0.58	0.1	2.8	2.64 2.38	3.61 3.35	3.8	3.1	1.7	0.2

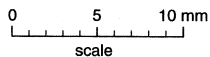
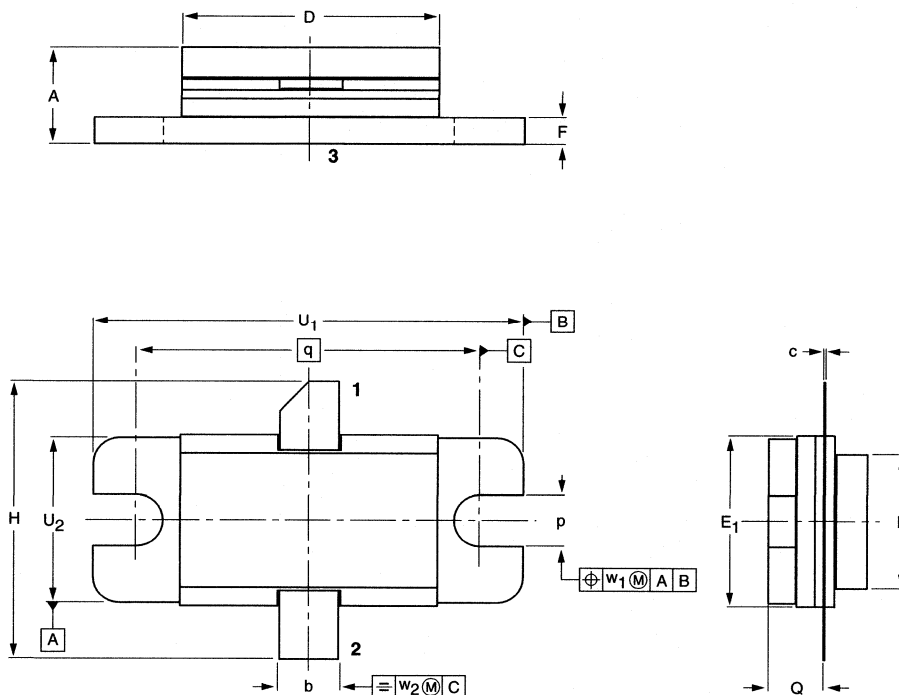
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT447A						97-02-28

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT448A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	E <sub>1</sub>	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	6.18 5.23	3.69 3.42	0.13 0.05	15.68 15.16	8.08 7.82	10.29 10.03	1.63 1.52	17.02 16.00	3.31 2.79	3.42 2.94	20.32	25.53 25.27	9.91 9.65	0.51	1.02

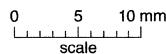
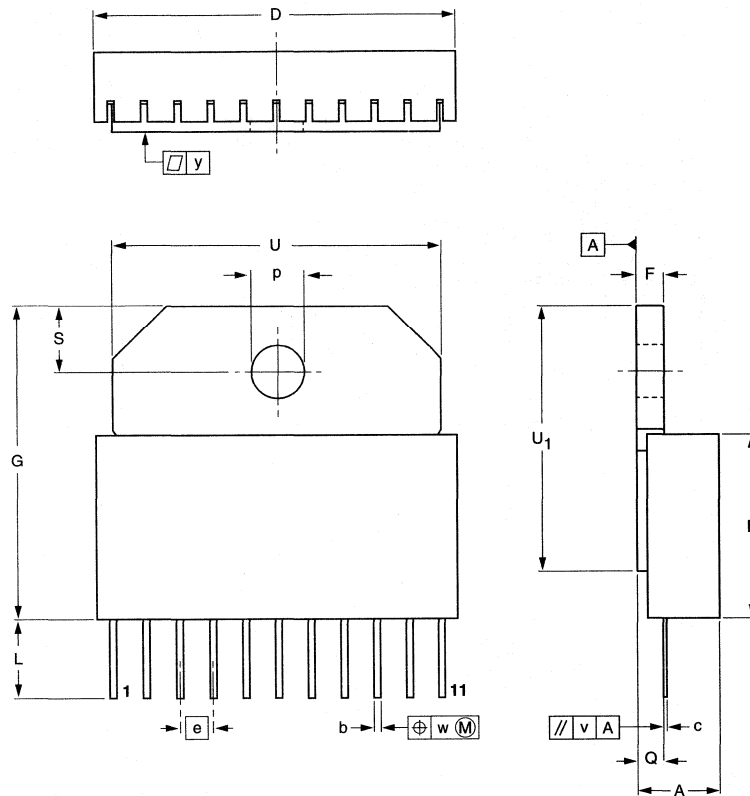
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT448A					97-05-29

Package outlines

Chapter 2

Ceramic single-ended flat package; heatsink mounted; 1 mounting hole;  
11 in-line gold-metallized leads

SOT451A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L	p	Q	S	U	U <sub>1</sub>	v	w	y
mm	5.9	0.56		28.3	13.9		2.2	23.8	6.2	4.2	2.0	5.2	25.4	20.4		0.25	0.1
	5.5	0.46	0.25	27.9	13.5	2.54	1.8	23.4	5.8	3.8	1.6	4.8	25.0	20.0	0.3		

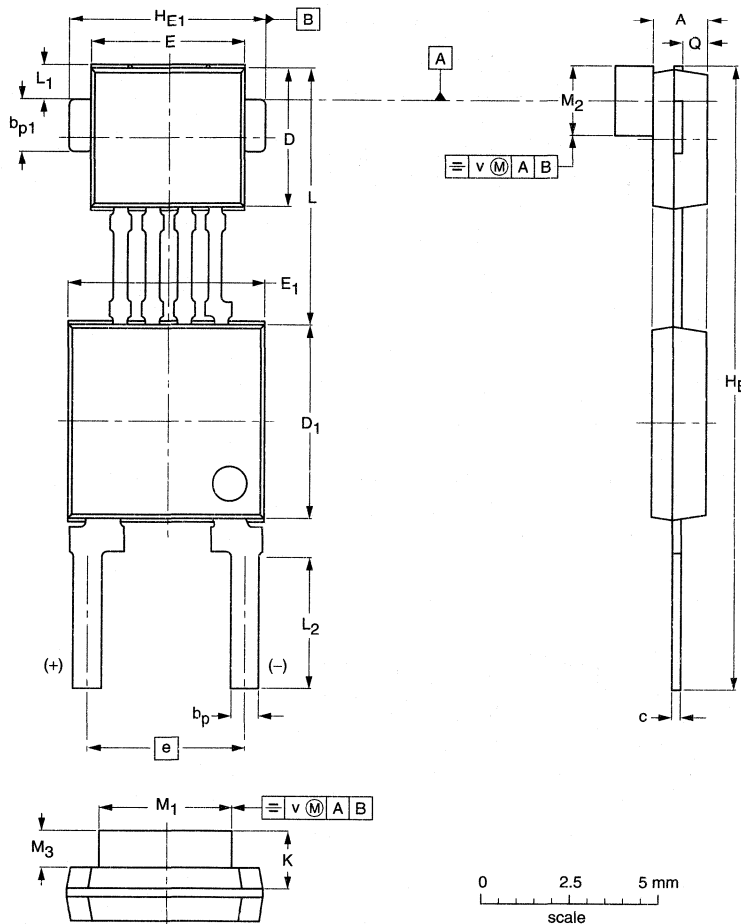
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT451A						97-06-26

Package outlines

Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (3.8 x 2.0 x 0.8 mm); 2 in-line leads

SOT453A



**DIMENSIONS (mm are the original dimensions)**

UNIT	A	b <sub>p</sub>	b <sub>p1</sub>	c	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H <sub>E</sub>	H <sub>E1</sub>	K max.	L	L <sub>1</sub>	L <sub>2</sub>	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	Q	v
mm	1.7 1.4	0.8 0.7	1.5 1.4	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	18.2 17.8	5.6 5.5	1.67	7.55 7.25	1.2 0.9	3.9 3.5	3.9 3.7	2.1 1.9	0.9 0.75	0.75 0.65	0.25

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT453A					96-11-12 97-02-28

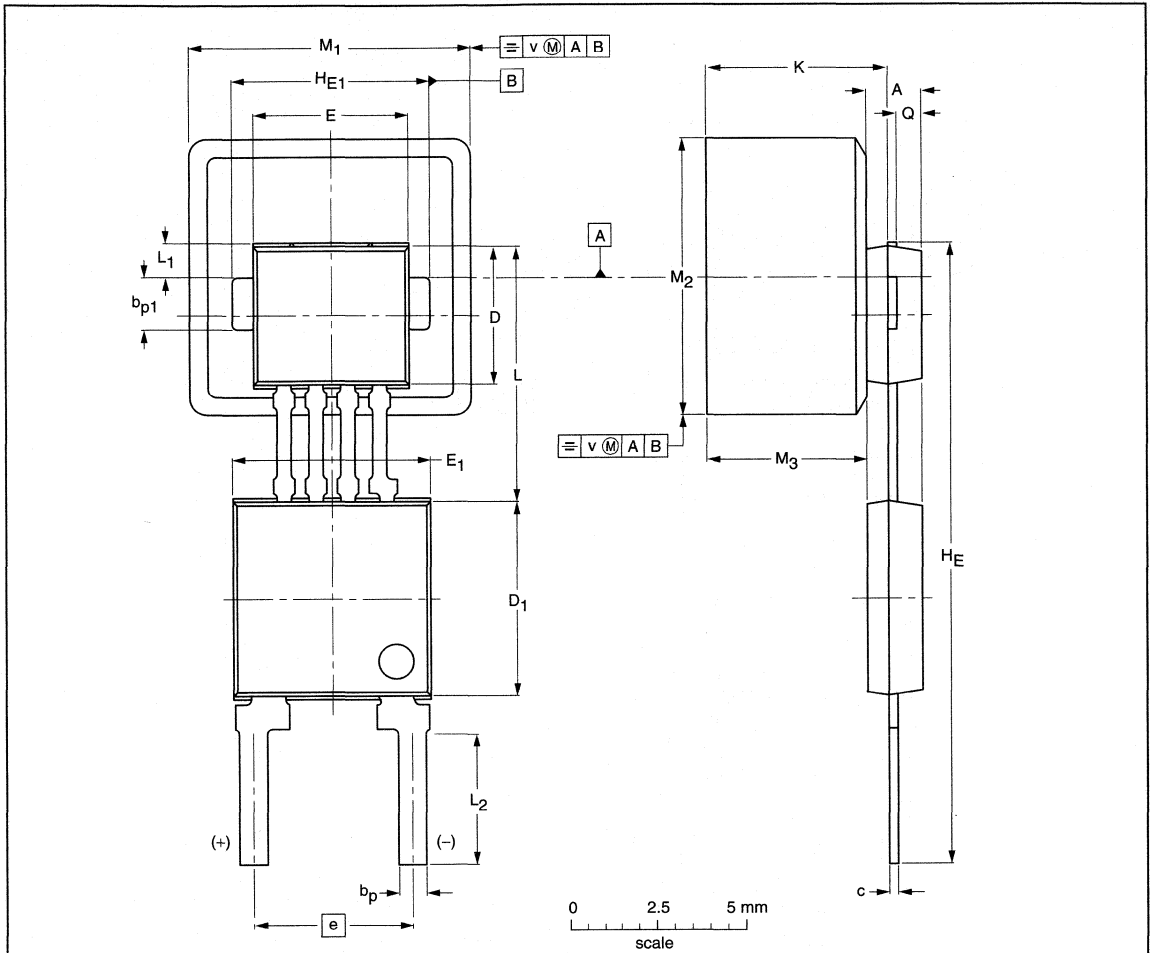


Package outlines

Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8.0 x 8.0 x 4.5 mm); 2 in-line leads

SOT453B



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	b <sub>p1</sub>	c	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H <sub>E</sub>	H <sub>E1</sub>	K <sub>max.</sub>	L	L <sub>1</sub>	L <sub>2</sub>	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	Q	v
mm	1.7 1.4	0.8 0.7	1.5 1.4	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	18.2 17.8	5.6 5.5	5.37	7.55 7.25	1.2 0.9	3.9 3.5	8.15 7.85	8.15 7.85	4.7 4.3	0.75 0.65	0.25

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

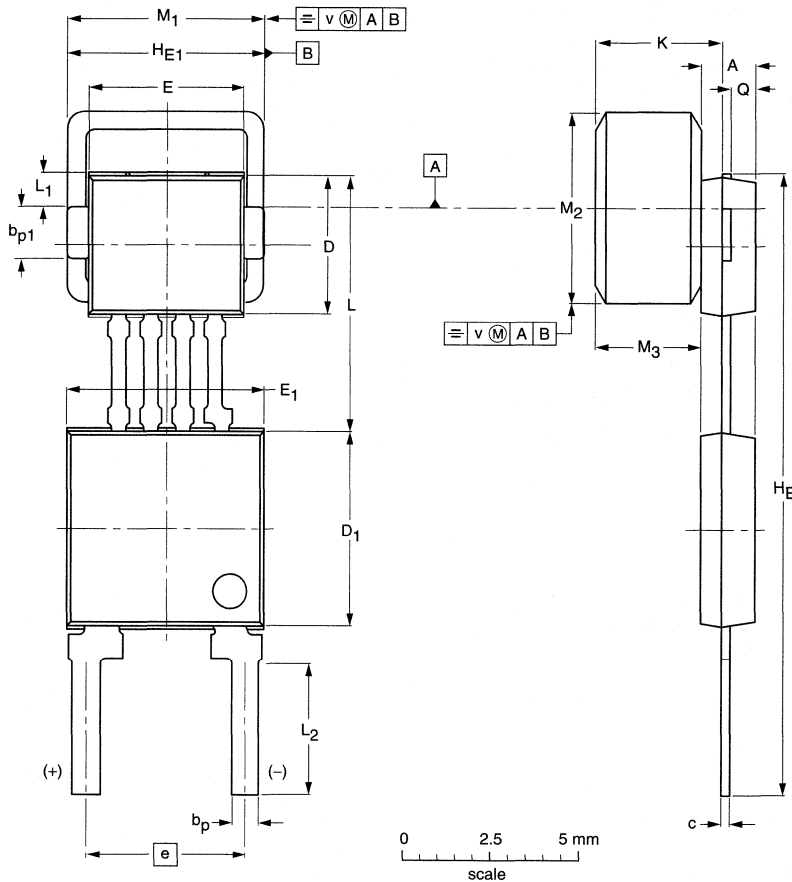
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT453B						96-11-12 97-02-28

Package outlines

Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 3.0 mm); 2 in-line leads

SOT453C



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>p</sub>	b <sub>p1</sub>	c	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H <sub>E</sub>	H <sub>E1</sub>	K max.	L	L <sub>1</sub>	L <sub>2</sub>	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	Q	v
mm	1.7	0.8	1.5	0.3	4.1	5.7	4.5	5.7	4.6	18.2	5.6	3.87	7.55	1.2	3.9	5.65	5.65	3.15	0.75	0.25
	1.4	0.7	1.4	0.24	3.9	5.5	4.3	5.5	4.4	17.8	5.5		7.25	0.9	3.5	5.35	5.35	2.85	0.65	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

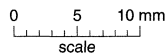
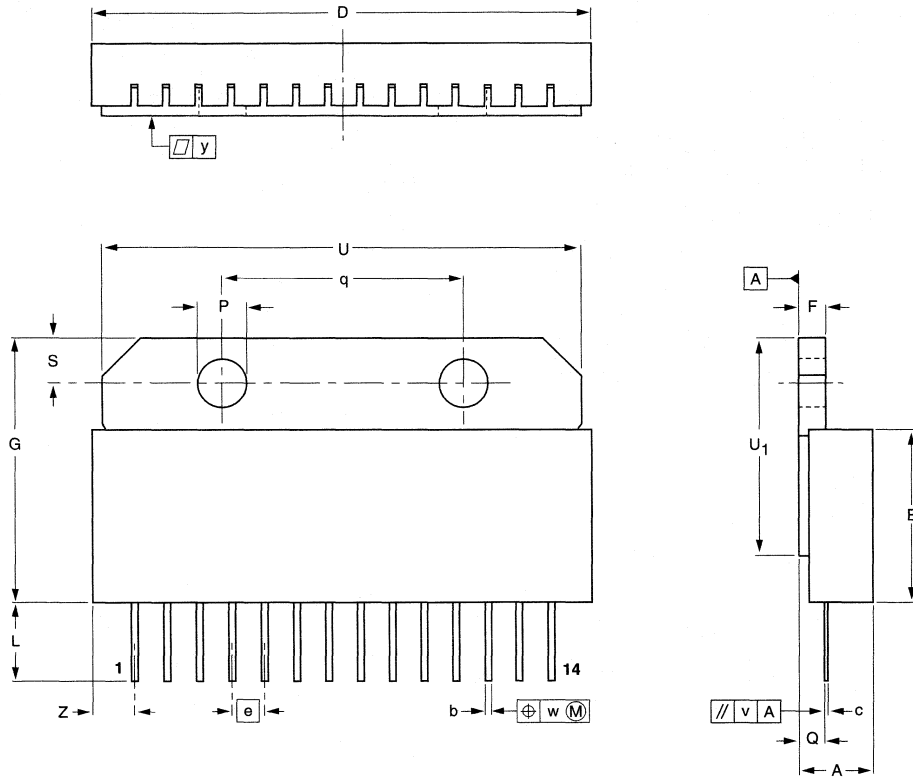
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT453C					96-11-12 97-02-28

Package outlines

Chapter 2

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes;  
14 in-line tin (Sn) plated leads

SOT454A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D max.	E	e	F	G max.	L min.	P	Q	q	S	U max.	U <sub>1</sub>	v	w	y	Z
mm	5.9 5.5	0.5	0.25	39.6	13.7	2.54	2.1 1.9	21.2	6	4.15 3.85	2.9 2.5	19	3.5	37.8	18.3	0.3	0.25	0.1	3.4 3.0

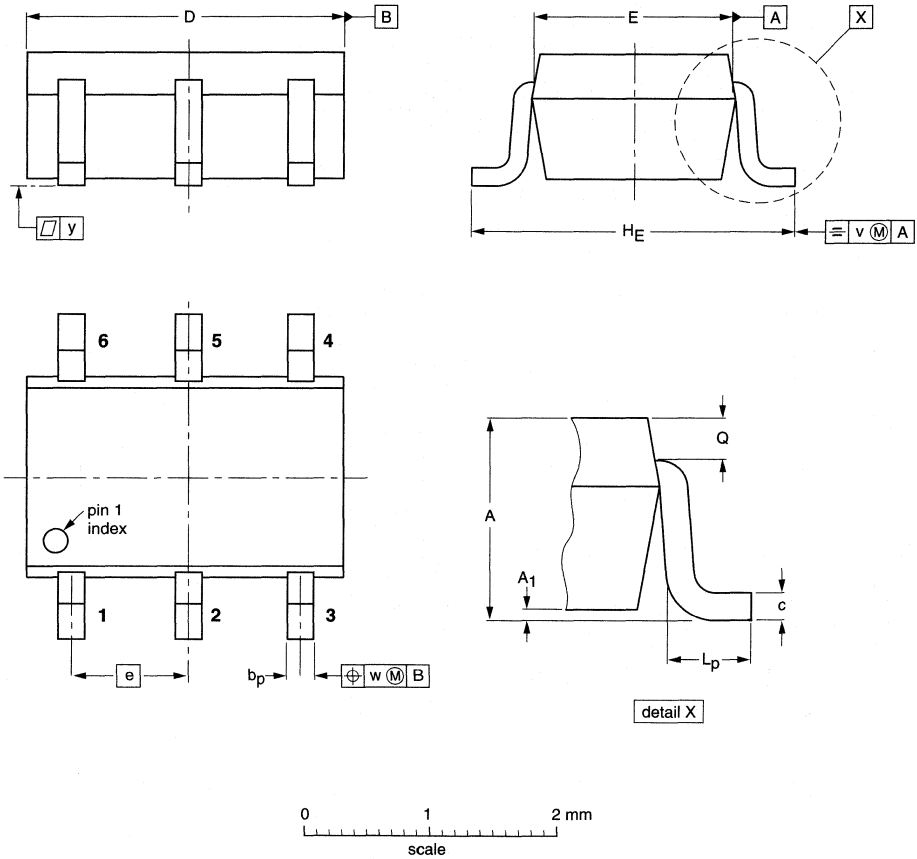
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT454A						97-07-01

Package outlines

Chapter 2

Plastic surface mounted package; 6 leads

SOT457



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

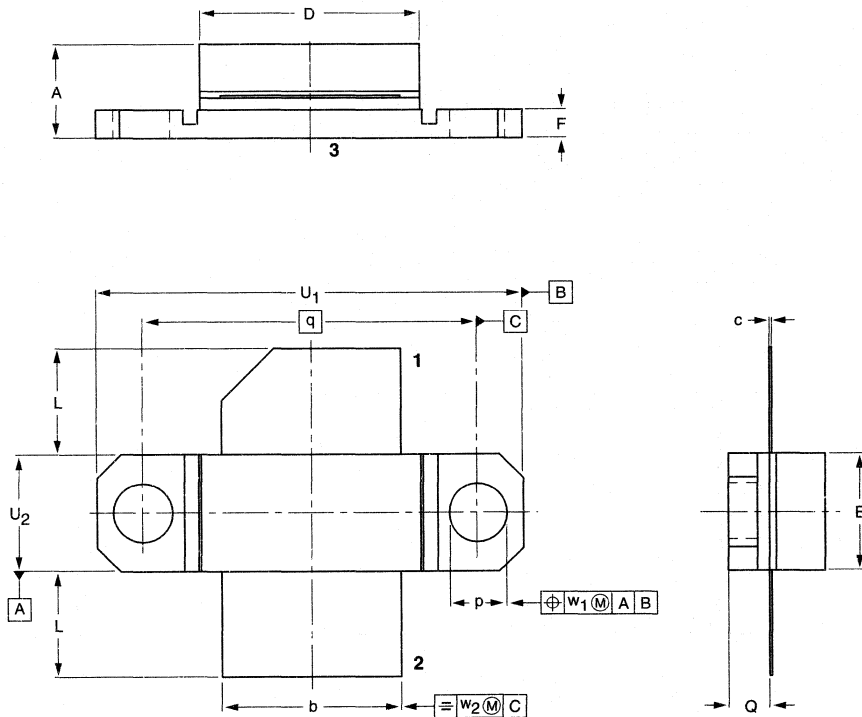
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT457			SC-74		97-02-28

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT460A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	L	p	Q	q	$U_1$	$U_2$	$w_1$	$w_2$
mm	5.39 4.49	9.78 9.52	0.16 0.07	12.45 11.68	6.94 6.22	1.66 1.39	6.10 5.33	3.28 3.02	2.37 1.95	17.98	22.99 22.73	6.43 6.17	0.51	1.02

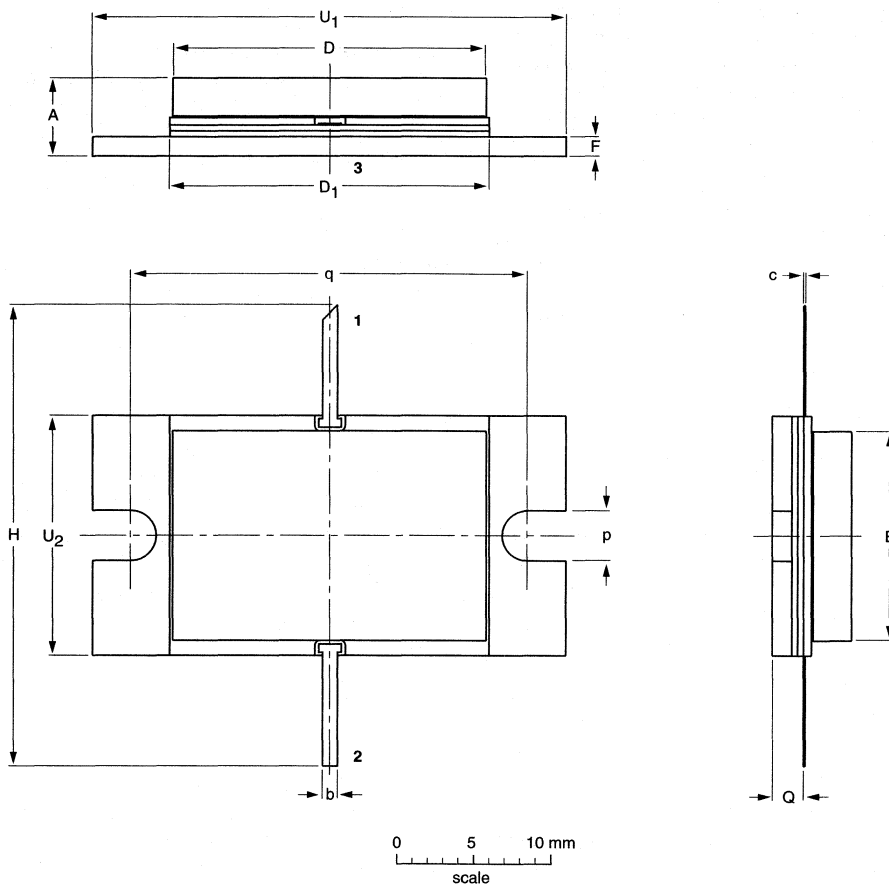
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT460A						97-05-23

Package outlines

Chapter 2

Flanged hermetic ceramic package; 2 mounting holes; 2 leads

SOT469A



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	F	H	p	Q	q	U <sub>1</sub>	U <sub>2</sub>
mm	5.73 4.53	1.12 0.86	0.13 0.07	20.76 20.44	21.11 20.85	13.95 13.63	1.40 1.14	30.61 30.35	3.43 3.17	2.16 1.90	26.14 25.88	31.12 30.86	15.93 15.67

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT469A					97-04-01

## Handling precautions

## Chapter 3

### ELECTROSTATIC CHARGES

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people (see Fig.1). The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of surrounding air.

Electrostatic discharge (ESD) is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All pins of Philips semiconductor devices are protected against electrostatic discharge. However we recommend that the following ESD precautions are complied with when handling such components.

### WORKSTATION FOR HANDLING ELECTROSTATIC-SENSITIVE DEVICES

Figure 1 shows a working area suitable for safely handling electrostatic-sensitive devices. It has a workbench, the surface of which is conductive and anti-static. The floor should also be covered with anti-static material.

The following precautions should be observed:

- Persons at a workbench should be earthed via a wrist strap and a resistor.
- All mains-powered equipment should be connected to the mains via an earth-leakage switch.
- Equipment cases should be grounded.
- Relative humidity should be maintained between 40% and 50%.
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail.
- Keep static materials, such as plastic envelopes and plastic trays etc., away from the workbench. If there are any such static materials on the workbench, remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) "*Protection of Electrostatic Sensitive Devices*", which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

### RECEIPT AND STORAGE OF COMPONENTS

Electrostatic-sensitive devices are packed for despatch in anti-static/conductive containers, usually boxes, tubes or blister tape. Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge.

Such devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any components that are stored temporarily should be packed in conductive or anti-static packing or carriers.

### PCB ASSEMBLY

Electrostatic-sensitive devices must be removed from their protective packing with grounded component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more components from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken. During assembly, ensure that the electrostatic-sensitive devices are the last of the components to be mounted and that this is done at a protected workstation.

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand-tools should be of conductive or anti-static material and, where possible, should not be insulated.

### TESTING PCBs

Completed PCBs must be tested at a protected workstation. Place the soldered side of the circuit board on conductive or anti-static foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the workbench. After testing, replace the PCB on the conductive foam to await packing.

Assembled circuit boards containing electrostatic-sensitive devices should always be handled in the same way as unmounted components. They should also carry warning labels and be packed in conductive or anti-static packing.

# Handling precautions

# Chapter 3

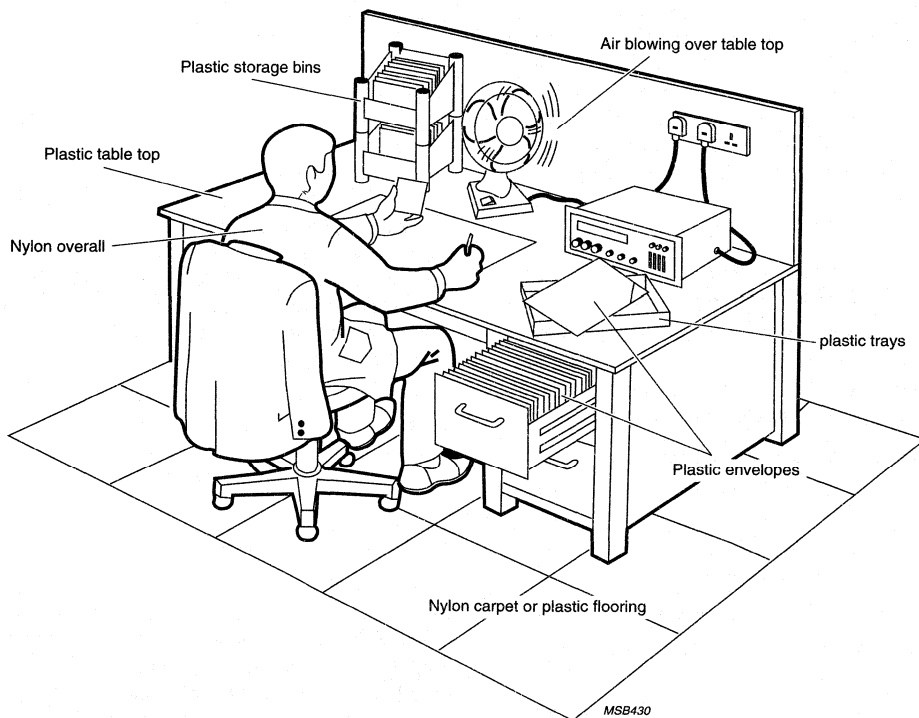


Fig.1 Typical working environment for electronic component handling showing potential ESD hazards.



Handling precautions

Chapter 3

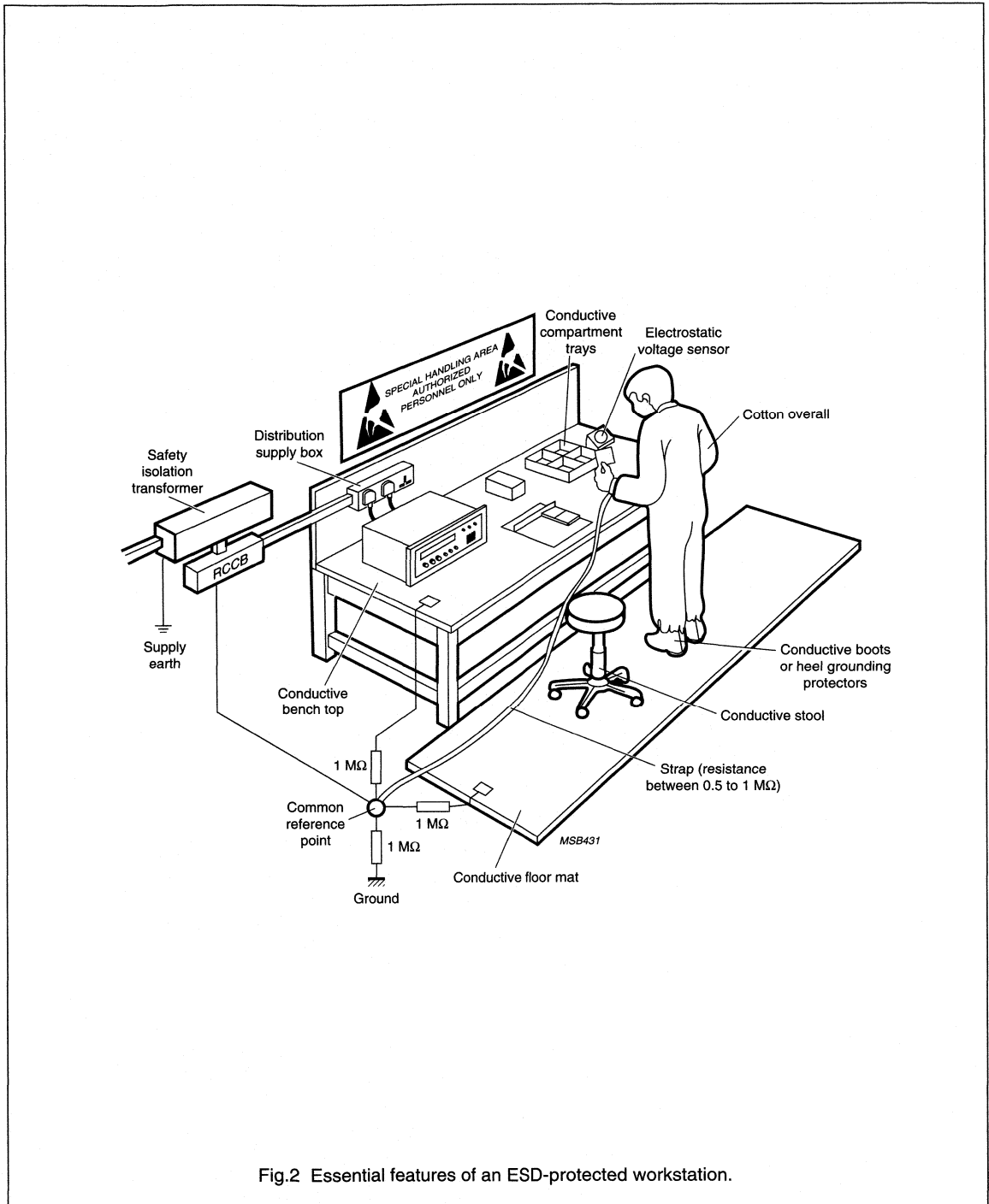


Fig.2 Essential features of an ESD-protected workstation.



# Soldering guidelines and SMD footprint design

## Chapter 4

### INTRODUCTION

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting. Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly.

### AXIAL AND RADIAL LEADED DEVICES

The following general rules are for the safe handling and soldering of axial and radial leaded diodes. Special rules for particular types may apply and, for these, instructions are given in the individual data sheets. With all components, excessive forces or heat can cause serious damage and should always be avoided.

#### Handling

- Avoid perpendicular forces on the body of the diode
- Avoid sudden forces on the leads or body. These forces are often much greater than allowed
- Avoid high acceleration as a result of any shock, e.g. dropping the device on a hard surface
- During bending, support the leads between body or stud and the bending point
- During the bending process, axial forces on the body must not exceed 20 N
- Bending the leads through 90° is allowed at any distance from the body when it is possible to support the leads during bending without contacting the body or weldings
- Bending close to the body or stud without supporting the leads is only allowed if the bend radius is greater than 0.5 mm
- Twisting the leads is allowed at any distance from the body or stud only if the lead is properly clamped between body or stud and the twisting point
- Without clamping, twisting the leads is allowed only at a distance of greater than 3 mm from the body; the torque angle must not exceed 30°
- Straightening bent leads is allowed only if the applied pulling force in the axial direction does not exceed 20 N and the total pull duration is not longer than 5 s.

#### Soldering

- Avoid any force on the body or leads during or immediately after soldering
- Do not correct the position of an already soldered device by pushing, pulling or twisting the body
- Avoid fast cooling after soldering.

The maximum allowable soldering time is determined by:

- Package type
- Mounting environment
- Soldering method
- Soldering temperature
- Distance between the point of soldering and the seal of the component body.

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The component may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the PCB has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### Mounting

If the rules for handling and soldering are observed, the following mounting or process methods are allowed:

- Preheating of the printed-wiring board before soldering up to a maximum of 100 °C
- Flat mounting with the diode body in direct contact with the printed-wiring board with or without metal tracks on both sides and/or plated-through holes
- Flat mounting with the diode body in direct contact with hot spots or hot tracks during soldering
- Upright mounting with the diode body in direct contact with the printed-wiring board if the body is not in contact with metal tracks or plated-through holes.

#### Repairing soldered joints

Apply the soldering iron to the component pin(s) below the seating plane, or not more than 2 mm above it. If the temperature of the soldering iron bit is below 300 °C, it may remain in contact for up to 10 s. If it is over 300 °C but below 400 °C, it may only remain in contact for up to 5 s.

# Soldering guidelines and SMD footprint design

## Chapter 4

### SURFACE-MOUNT DEVICES

Since the introduction of surface mount devices (SMDs), component design and manufacturing techniques have changed almost beyond recognition. Smaller pitch, minimum footprint area and reduced component volume all contribute to a more compact circuit assembly. As a consequence, when designing PCBs, the dimensions of the footprints are perhaps more crucial than ever before.

One of the first steps in this design process is to consider which soldering method, either wave or reflow, will be used during production. This determines not only the solder footprint dimensions, but also the minimum spacing between components, the available area underneath the component where tracks may be laid, and possibly the required component orientation during soldering.

Although reflow soldering is recommended for SMDs, many manufacturers use, and will continue to use for some time to come, a mixture of surface-mount and through-hole components on one substrate (a mixed print).

The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

To help with your circuit board design, this guideline gives an overview of both reflow and wave soldering methods, and is followed by some useful hints on hand soldering for repair purposes, and the recommended footprints for our SMD discrete semiconductor packages.

### Reflow soldering process

There are three basic process steps for single-sided PCB reflow soldering, these are:

1. Applying solder paste to the PCB
2. Component placement
3. Reflow soldering.

#### APPLYING SOLDER PASTE TO THE PCB

Solder paste can be applied to the PCBs solder lands by one of either three methods: dispensing, screen or stencil printing.

Dispensing is flexible but is slow, and only suitable for pitches of 0.65 mm and above.

With screen printing, a fine-mesh screen is placed over the PCB and the solder paste is forced through the mesh onto the solder lands of the PCB. However, because of mesh aperture limitations (emulsion resolution), this method is only suitable for solder paste deposits of 300  $\mu\text{m}$  and wider.

Stencil printing is similar to screen printing, except that a metal stencil is used instead of a fine-mesh screen. The stencil is usually made of stainless steel or bronze and should be 150 to 200  $\mu\text{m}$  thick. A squeegee is passed across the stencil to force solder paste through the apertures in the stencil and onto the solder lands on the PCB (see Fig.1). It does not suffer from the same limitations as the other two printing methods and so is the preferred method currently available.

It is recommended that for solder paste printing, the equipment is located in a controlled environment maintained at a temperature of  $23 \pm 2$  °C, and a relative humidity between 45% and 75%.

# Soldering guidelines and SMD footprint design

## Chapter 4

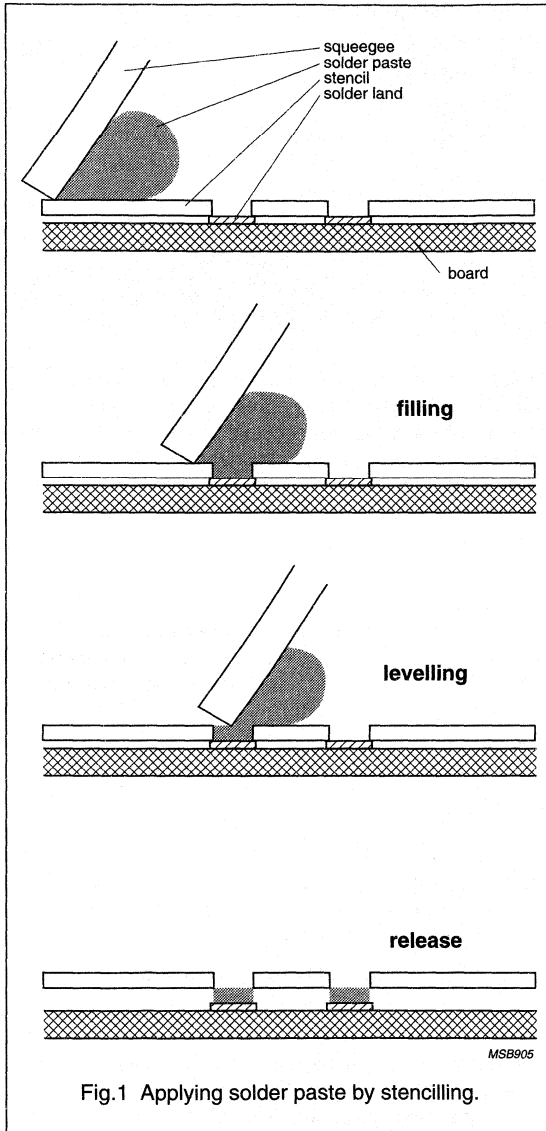


Fig.1 Applying solder paste by stenciling.

The amount of solder paste used must be sufficient to give reliable soldered joints. This amount is controlled by the stencil thickness, aperture dimensions, process settings, and the volume of paste pressed through the apertures by the squeegee.

The downward force of the squeegee is counteracted by the hydrodynamic pressure of the paste, and so the machine should be set to ensure that the stencil is just 'cleaned' by the squeegee.

Suitable aperture dimensions depend on the stencil thickness. The solder paste deposits must have a flat part on the top (Fig.2, examples 4 and 5), which can be achieved by correct process settings. The footprints given in this book were designed for these correct deposit types. Stencil apertures that are too small result in irregular dots on the lands (Fig.2, examples 1 to 3). If the apertures are too large, solder paste can be scooped out, particularly if a rubber squeegee is used (Fig.2, example 6).

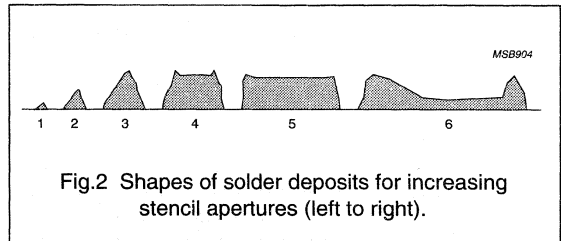


Fig.2 Shapes of solder deposits for increasing stencil apertures (left to right).

Ideally, the deposited solder paste should sit entirely on the solder land. The tolerated misplacement of solder paste with respect to the solder land is determined by the most critical component. The solder paste deposit must be deposited within 100 µm with respect to the solder land.

Furthermore, the tackiness (tack strength) of the solder paste must be sufficient to hold surface-mount devices on the PCB during assembly and during transport to the reflow oven. Tack strength depends on factors such as paste composition, drying conditions, placement pressure, dwell time and contact area. As a general rule, component placement should be within four hours after the paste printing process.

### Squeegee

The squeegee can be either metal or rubber. A metal squeegee gives better overall results and so is recommended, however with step stencils, a rubber squeegee has to be used. The footprints given in this chapter were designed for application by both types of squeegee.

### Stencil printing

The printing process must be able to apply the solder paste deposits to the PCB:

- In the correct amounts
- At the correct position on the lands
- With an acceptable height and shape.

# Soldering guidelines and SMD footprint design

## Chapter 4

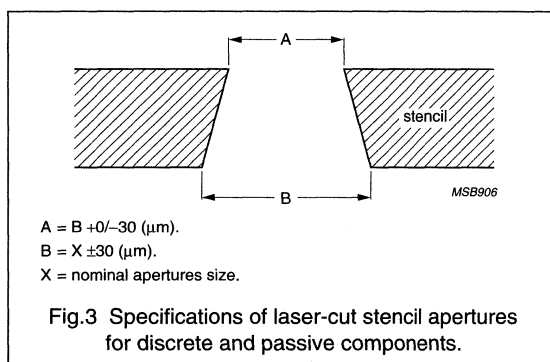
### Stencil apertures

Stencil apertures can be made by either:

- Etching
- Laser cutting
- Electroforming.

Of the three methods, etching is less accurate as the deviation in aperture dimensions with respect to the target is relatively large (target is  $+50\ \mu\text{m}$  at squeegee side and  $0\ \mu\text{m}$  at PCB side).

Laser-cut and electroformed stencils have smaller deviations in dimensions and are therefore more suitable for small and fine-pitch components (see Fig.3).



A useful method of controlling the stencil printing process during production is by monitoring the weight of solder paste on the board which may vary between 80% and 110% of the theoretical amount according to the target (designed) apertures. Smearing and clogging of a small aperture cannot be detected with this method.

### Solder paste

Reflow soldering uses a paste consisting of small nodules of solder and a flux with binder, solvents and additives to control rheological properties. The flux in the solder paste can be rosin mildly activated or rosin activated.

The requirements of the solder paste are:

- Good rolling behaviour
- No slump during heat-up
- Low viscosity during printing
- High viscosity after printing
- Sufficient tackiness to hold the components
- Removal of oxides during reflow soldering.

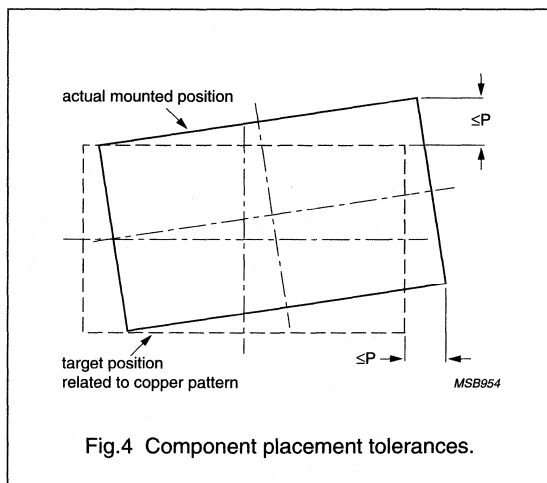
Suitable solder paste types have the following compositions:

- Sn62Pb36Ag2
- Sn63Pb37
- Sn60Pb40.

### COMPONENT PLACEMENT

The position of the component with respect to the solder lands is an important factor in the final result of the assembly process. A misaligned component can lead to unreliable joints, open circuits and/or bridges between leads.

The placement accuracy is defined as the maximum permissible deviation of the component outline or component leads, with respect to the actual position of the solder land pattern belonging to that component or component leads on the circuit board (see Fig.4).



A maximum placement deviation ( $P$ ) of  $0.25\ \text{mm}$  is used in these guidelines, which relates to the accuracy of a low-end placement machine. A higher placement accuracy is required for components with a fine pitch. This is given in the footprint description for the components concerned.

Besides the position in x- and y-directions, the z-position with respect to the solder paste, which is determined by the placement force, is also important. If the placement force is too high, solder paste will be squeezed out and solder balls or bridges will be formed. If the force is too low, physical contact will be insufficient, leads will not be soldered properly and the component may shift.

## Soldering guidelines and SMD footprint design

## Chapter 4

### REFLOW SOLDERING

There are several methods available to provide the heat to reflow the solder paste, such as convection, hot belt, hot gas, vapour phase and resistance soldering. The preferred method is, however, convection reflow.

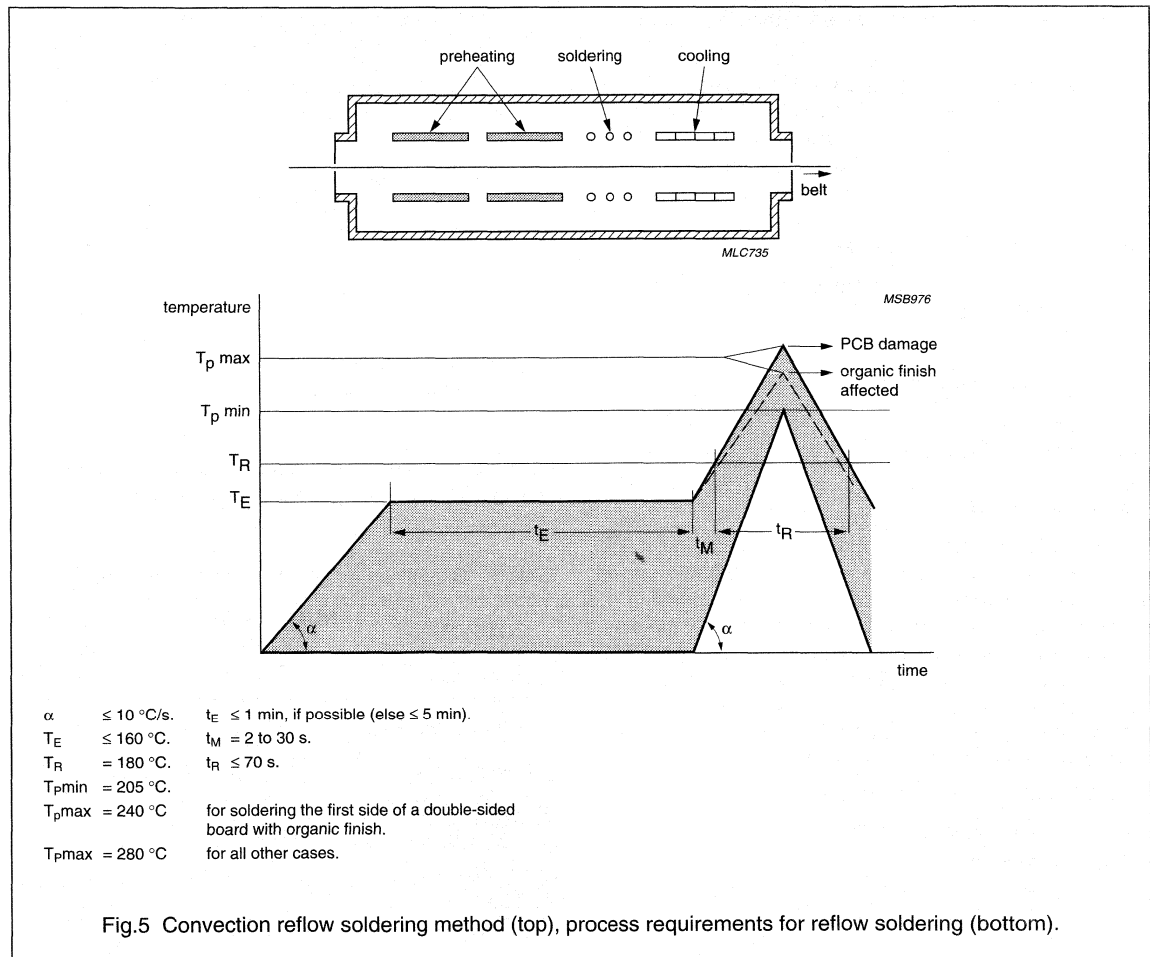
#### Convection reflow

With this method, the PCBs pass through an oven where it is preheated, reflow soldered and cooled (see Fig.5). If the heating rate of the board and components are similar, however, preheating is not necessary.

During the reflow soldering process, all parts of the board must be subjected to an accurate temperature/ time profile. Figure 5 shows a suitable profile framework for

single-sided reflow soldering and the first side of double-sided print boards. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

Reflow soldering can be done in either air or a nitrogen atmosphere. If soldering in air, the temperature ( $T_p$ ) must not exceed 240 °C on the first side of a double-sided print board with organic coated solder lands. This is because peak temperatures greater than 240 °C reduce the solderability of the lands on the second side to be soldered. This peak temperature can rise to 280 °C when soldering the second side with organic coated solder lands in air.



# Soldering guidelines and SMD footprint design

## Chapter 4

If soldering in a nitrogen atmosphere, a peak temperature of 280 °C is allowed for double-sided print boards or single-sided reflow soldering. Soldering in a nitrogen atmosphere results in smoother joint meniscus, smaller contact angles, and better wetting of the copper solder lands.

The profile can be achieved by correct combinations of conveyor speed and heater temperature. To check whether the profile is within specification, the coldest and hottest spots on the board have to be located.

To do this, you should dispense solder paste deposits regularly over the surface of a test board and on the component leads. Set the oven to a moderate temperature with maximum conveyor velocity and pass the test board through. If too many solder paste dots melt, lower the oven's temperature. Continue passing test boards through the oven, while lowering the speed of the belt in small steps.

The deposit that melts first indicates the warmest location, the one that melts last indicates the coldest location. Paste dots not reflowed after two runs must be replaced by fresh dots. Thermocouples have to be mounted at the coldest and warmest location and temperature profiles measured.

### Double-wave soldering process

There are four basic process steps for double-wave soldering, these are:

1. Applying adhesive
2. Component placement
3. Curing adhesive
4. Wave soldering process.

#### APPLYING ADHESIVE

To hold SMDs on the board during wave soldering, it is necessary to bond the component to the PCB with one or more adhesive dots. This is done either by dispensing, stencilling or pin transfer. Dispensing is currently the most popular technique. It is flexible and allows a controlled amount of adhesive to be applied at each position. Stencil printing and pin transfer are less flexible and are mainly used for mass production. The component-specific requirements for an adhesive dot are:

- Shape (volume) of the adhesive dot
- Number of dots per component
- Position of the dots.

#### Volume of adhesive

There must be enough adhesive to keep components in their correct positions while being transported to the curing oven. This means that the deposited adhesive must be higher than the gap between the component and the board surface. Nevertheless, there should not be too much deposit as it may smear onto the solder lands, where it can affect their solderability. The gap between a component and printed board depends on the geometry of the board and component (see Fig.6).

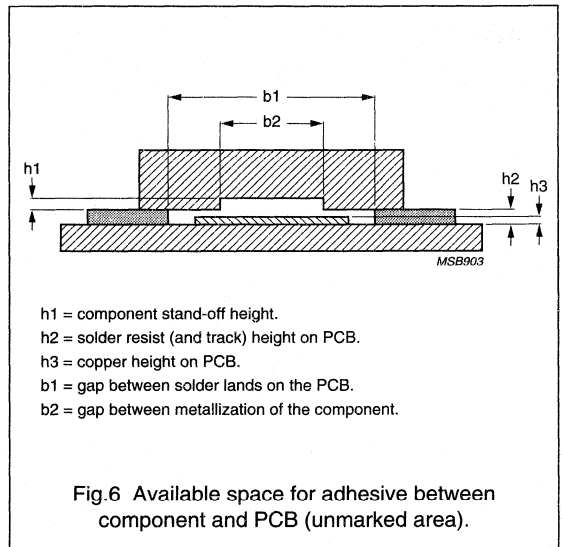


Table 1 gives guidelines for volumes of adhesive dots per package. The spreading in volumes should be within  $\pm 15\%$ .

**Table 1** Guidelines for volumes of adhesive dots

COMPONENT	NUMBER OF DOTS	VOLUME PER DOT (mm <sup>3</sup> )
SOD106(A)	1	0.65
SOD80(C), SOD87	1	0.5
	2	0.08
SOD110, SOD323	2	0.065
SOT323 (SC70-3)	2	0.045
SOT23, SOT143, SOT 346 (SC59)	2	0.06
SOT89	2	0.3
SOT223	2	0.70



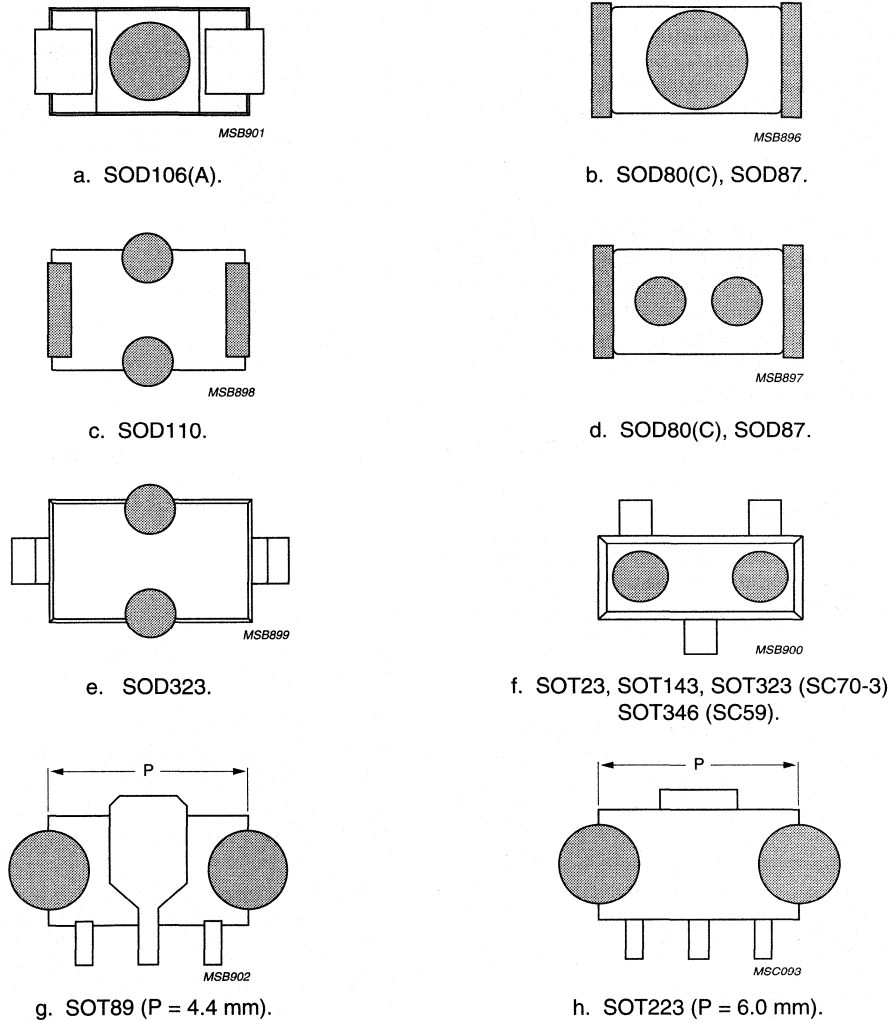
# Soldering guidelines and SMD footprint design

## Chapter 4

### Number, position and volume of dots per component

Figure 7 shows the recommended positions and numbers of adhesive dots for a variety of packages. SOD106(A), SOT89 and SOT223 packages require much larger

adhesive dots compared with those for other components. SOD80(C) and SOD87 packages can have one large adhesive dot (recommended) or two smaller adhesive dots.



For optimum power dissipation, the SOT89 requires a good thermal contact (i.e. good solder joint) between the package and the solder land. During wave-soldering, however, flux may not always reach the total soldering area beneath the component body, which in turn can lead to an incomplete solder joint. If the SOT89 is double-wave soldered, therefore, power derating must be applied.

Fig.7 Position of adhesive dots. Pitch between two small dots is 1.0 mm.

# Soldering guidelines and SMD footprint design

## Chapter 4

### Nozzle outlet diameter

Depending on adhesive type and component size, the nozzle outlet diameter of the dispenser can vary between 0.6 and 0.7 mm for the larger dots, and between 0.3 and 0.5 mm for the smaller dots.

As the rheology of the adhesive is temperature dependent, the temperature in the nozzle must be carefully controlled before dispensing. The required temperature depends on the adhesive type, but is usually between 26 °C and 32 °C to maintain the adhesive's rheology within specification during dispensing. Thermally curing epoxy adhesives are normally used.

### Adhesives

Beside the nozzle diameters, different adhesive types are also used for different component sizes. Small components can be secured during assembly and wave soldering with a thin (low green strength) adhesive, which can be dispensed at high speeds. For larger components (such as QFP and SO packages), a higher green strength adhesive is required.

### COMPONENT PLACEMENT

Positioning components on the PCB is similar in practice to that of reflow soldering.

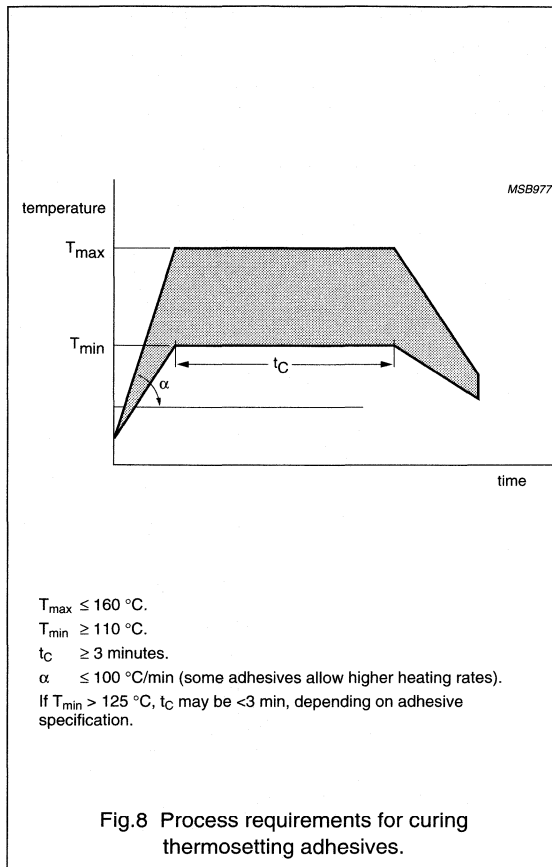
To prevent component shift and smearing of the adhesive, board support is important while placing components. This is particularly important when placing the SOD106(A) package.

### CURING THE ADHESIVE

To provide sufficient bonding strength between component and board, the adhesive must be properly cured. Figure 8 gives general process requirements for curing most thermosetting epoxy adhesives with latent hardeners. The temperature profile of all adhesive dots on the PCB must be within this framework. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

To check whether the profile is within specification, the temperature of coldest and hottest spots must be measured. The coldest spot is usually under the largest package: the hottest spot is usually under the smallest package.

The adhesive can be cured either by infrared or hot-air convection.



### Bonding strength

The bonding strength of glued components on the board can be checked by measuring the torque force. For small components the requirements are given in Table 2. No values are specified for larger packages.

**Table 2** Bonding strength requirements

COMPONENT	MINIMUM BONDING STRENGTH (cNcm)	TARGET BONDING STRENGTH (cNcm)
SOD323, SOD110, SOT323 (SC70-3)	110	250
SOD80(C), SOD87	200	350
SOT23, SOT346 (SC59), SOT143	150	250

## Soldering guidelines and SMD footprint design

## Chapter 4

### WAVE SOLDERING PROCESS

After applying adhesive, placing the component on the PCB and curing, the PCB can be wave soldered. The wave soldering process is basically built up from three sub-processes. These are:

1. Fluxing
2. Preheating
3. (Double) wave soldering.

Although listed here as sub-process they are in practice combined in one machine. All are served by one transport mechanism, which guides the PCBs at an incline through the soldering machine. It's important to note that the PCB must be loaded into the machine so that the SMDs on the board come into direct contact with the solder wave (see Fig.9).

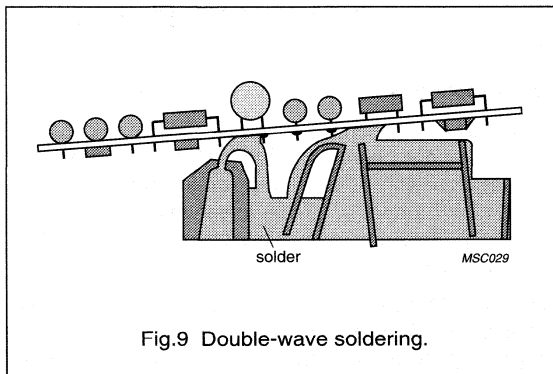


Fig.9 Double-wave soldering.

In principle, two different systems of PCB transports are available for wave soldering:

- **Carrier transport**  
PCBs are mounted on a soldering carrier, which moves through the soldering machine, taking it from one sub-process to the next. The advantage of carrier mounting is that the board is fixed and warpage during soldering is reduced.
- **Carrierless transport**  
PCBs are guided through the soldering machine by a chain with grips. This method is more convenient for mass production.

### Fluxing

Fluxing is necessary to promote wetting both of the PCB and the mounted components. This ensures a good and even solder joint.

During the fluxing process, the solder side of the PCB (including the components) are covered with a thin layer of solder flux, which can be applied to the PCB either by spraying or as a foam. Although several types of solder flux are available for this purpose, they can be categorized into three main groups:

- Non-activated flux (e.g. rosin-based fluxes)
- Mildly activated flux (e.g. rosin-based or synthetic fluxes)
- Highly activated flux (e.g. water-soluble fluxes).

The choice for a particular flux type depends mainly on the products to be soldered.

Although there is always some flux residue left on the PCB after soldering, it's not always necessary to wash the boards to remove it. Whether to clean the board can depend on:

- The type of flux used (highly activated fluxes are corrosive and so should always be removed).
- The required appearance of the board after soldering.
- Customer requirements.

### Preheating

After the flux is applied, the PCB needs to be preheated. This serves several purposes: it evaporates the flux solvents, it accelerates the activity of the flux and it heats the PCB and components to reduce thermal shock.

The required pre-heat temperature depends on the type of flux used. For example, the more common low-residue fluxes require a pre-heat temperature of 120 °C (measured on the wave solder side of the PCB).

### (Double) wave soldering

The PCB first passes over a highly intensive (jet) solder wave with a carefully controlled constant height. This ensures good contact with the PCB, the edges of SMDs and the leads of components near to high non-wetted bodies. The greater the board's immersion depth into this first wave, the fewer joints will be missed.

If the PCB is carrier mounted, the first wave's height, and thus the board's immersion depth, can be greater. Carrierless soldering is more convenient for mass production, but the height of the wave must be lower to avoid solder overflowing to the top side of the board. The height of the jet wave is given in Table 3 along with an indication of soldering process window. This information is based on a 1.6 mm thick PCB.

## Soldering guidelines and SMD footprint design

## Chapter 4

**Table 3** Process ranges for carrierless and carrier double wave soldering

	CARRIERLESS	CARRIER
Preheat temperature of board at wave solder side (°C)	120 ±10	
Heating rate preheating (°C/s)	$\Delta T/\Delta t \leq 3$	
First (jet) wave: wave height with respect to bottom side of board (mm)	1.6 +0.5/-0	3.0 +0.5/-0
Second (laminar) wave (double sided overflow): height with respect to underside of the board (mm) relative stream velocity with respect to the board	0.8 +0.5/-0 0	
Solder temperature (°C)	250 ±3	
Contact times (s): first (jet) wave second (laminar) wave	0.5 +0.5/-0 2.0 ±0.2 (plain holes); 2.5 ±0.2 (plated holes)	
PCB transport angle (°)	7 ±0.5	
Solder alloys	Sn60Pb40; Sn60Pb38Bi2	

The second, smoother laminar solder wave completes formation of the solder fillet, giving an optimal soldered connection between component and PCB. It also reduces the possibility of solder bridging by taking up excessive solder.

To reduce lead/tin oxides and possibly other solder imperfection forming during soldering, the complete wave configuration can be encapsulated by an inert atmosphere such as nitrogen.

### Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component package could be damaged by the iron.

### Assessment of soldered joint quality

The quality of a soldered joint is assessed by inspecting the shape and appearance of the joint. This inspection is normally done with either a low-powered magnifier or microscope, however where ultra-high reliability is required, video, X-ray or laser inspection equipment may be considered.

Both sides of the PCB should be carefully examined: there should be no misaligned, missing or damaged components, soldered joints should be clean and have a similar appearance, there should be no solder bridging or residue, and the PCB should be assessed for general cleanliness.

Unlike leaded component joints where the lead also provides added mechanical strength, the SMD relies on the quality of the soldering for both electrical and mechanical integrity. It is therefore necessary that the inspector is trained to make a visual assessment with regard to long-term reliability.

Criteria used to assess the quality of an SMD solder joint include:

- Correct position of the component on the solder lands
- Good wetting of the surfaces
- Correct amount of solder
- A sound, smooth joint surface.

# Soldering guidelines and SMD footprint design

## Chapter 4

### POSITIONING

If a lead projects over the solder land too far an unreliable joint is obtained. Figures 10 to 12 show the maximum shift allowed for various components. The dimensions of these solder lands guarantee that, in the statistically extreme situation, a reliable soldered joint can be made.

### GOOD WETTING

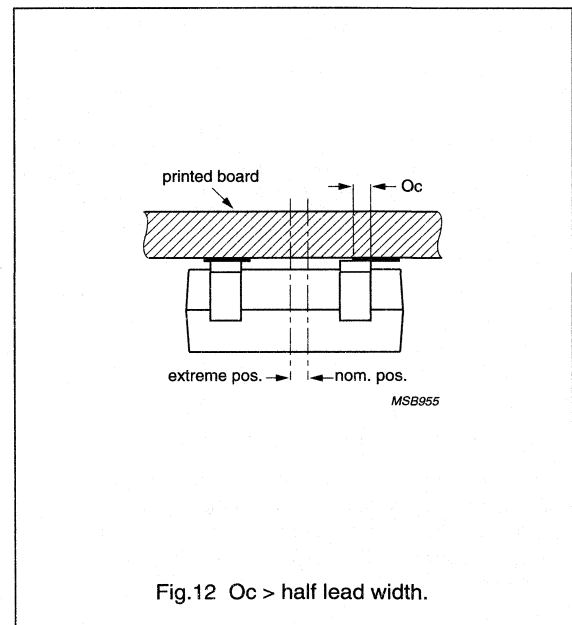
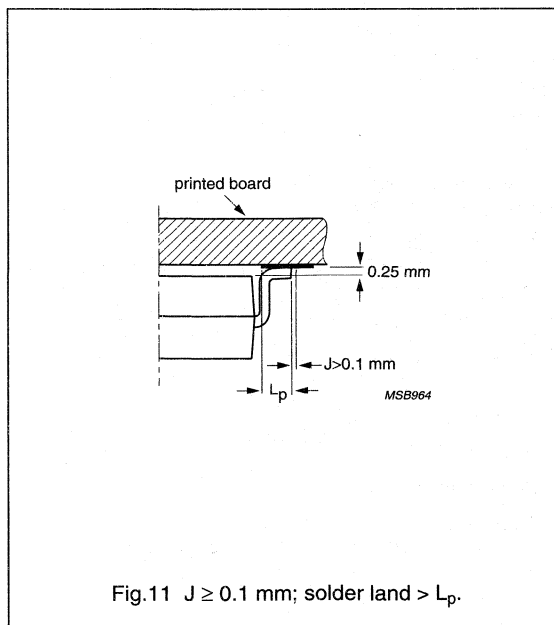
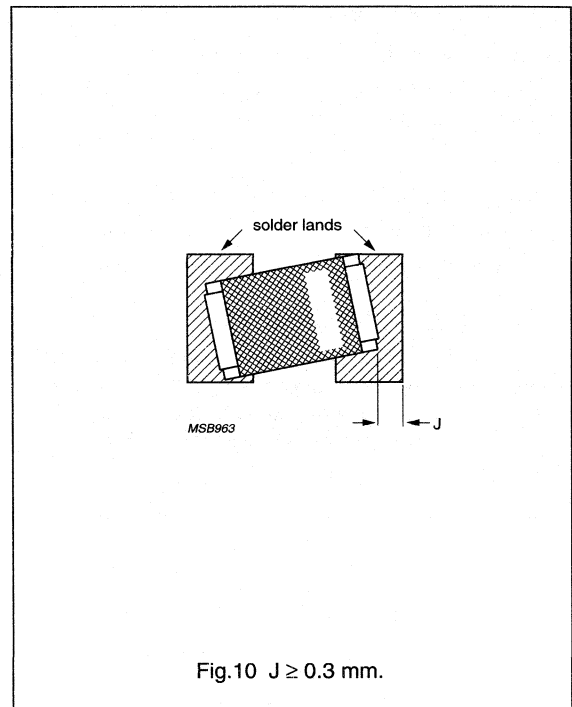
This produces an even flow of solder over the surface land and component lead, and thinning towards the edges of the joint. The metallic interaction that takes place during soldering should give a smooth, unbroken, adherent layer of solder on the joint.

### CORRECT AMOUNT OF SOLDER

A good soldered joint should have neither too much nor too little solder: there should be enough solder to ensure electrical and mechanical integrity, but not so much that it causes solder bridging.

### SOUND, SMOOTH JOINT SURFACE

The surface of the solder should be smooth and continuous. Small irregularities on the solder surface are acceptable, but cracks are unacceptable.



# Soldering guidelines and SMD footprint design

## Chapter 4

### Footprint definitions

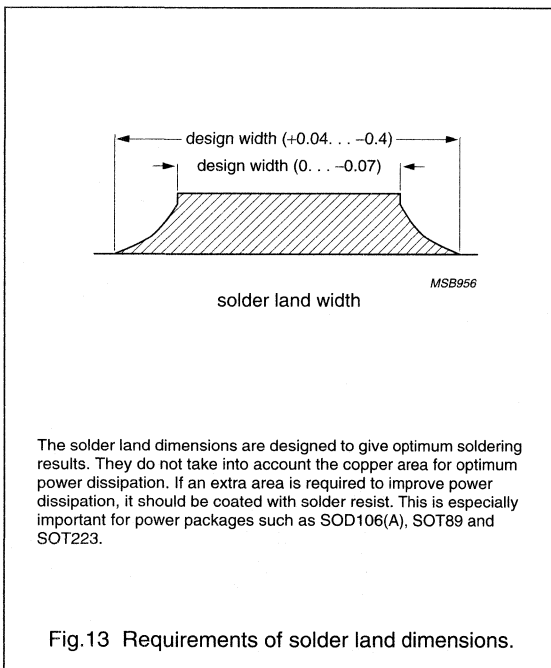
A typical SMD footprint, is composed of:

- Solder lands (conductive pattern)
- Solder resist pattern
- Occupied area of the component
- Solder paste pattern (for reflow soldering only)
- Area underneath the SMD available for tracks
- Component orientation during wave soldering.

#### SOLDER LANDS (CONDUCTIVE PATTERN)

The dimensions of the solder lands given in these guidelines are the actual dimensions of the conductive pattern on the printed board (see Fig.13).

These dimensions are more crucial for fine-pitch components.



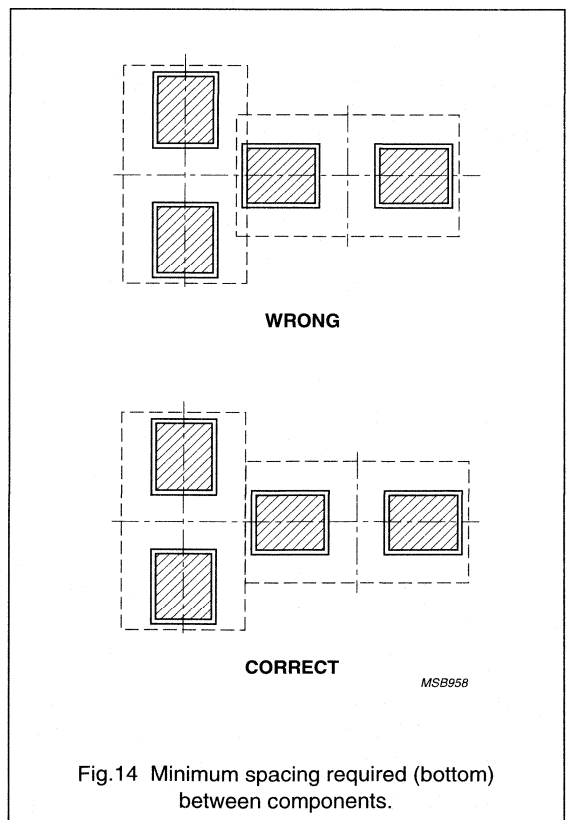
#### SOLDER RESIST PATTERN

The solder resist on the circuit board prevents short circuits during soldering, increases the insulation resistance between adjacent circuit details and stops solder flowing away from solder lands during reflow soldering.

In contrast to the tracks, which must be entirely covered, solder lands must be free of solder resist. Because of this, the cut-outs in the solder resist pattern should be at least 0.15 mm or 0.3 mm larger than the relevant solder lands (for a photo-defined and screen printed solder resist pattern respectively). The solder resist cut-outs given with the footprints in these guidelines are sketched and their dimensions can be calculated by using the above rule. Consult your printed board supplier for agreement with these solder resist cut-outs.

#### OCCUPIED AREA OF THE COMPONENT

A minimum spacing between components is necessary to avoid component placement problems, short circuits during wave or reflow soldering and dry solder joints during wave soldering caused by non-wettable component bodies. These problems can be avoided by placing the components so the occupied areas do not overlap (see Fig.14).



# Soldering guidelines and SMD footprint design

## Chapter 4

### SOLDER PASTE PATTERN

It is important to use a solder paste printer which is optical aligned with the PCBs copper pattern for the reflow footprints presented here. This is because, for these footprints, the solder paste deposit must be within a 0.1 mm tolerance with respect to the copper pattern.

To ensure the right amount of solder for each solder joint, the stencil apertures must be equal to the solder paste areas given by the footprints.

### AREA AVAILABLE FOR TRACKS (CONDUCTIVE PATTERN)

Tracks underneath leadless SMDs must be covered with solder resist. However, as solder resist can sometimes be thin or have pin holes at the edges of tracks (especially when applied by screen printing), an additional clearance for tracks with respect to the actual metallization position of the mounted component should be taken into account (see Fig.15).

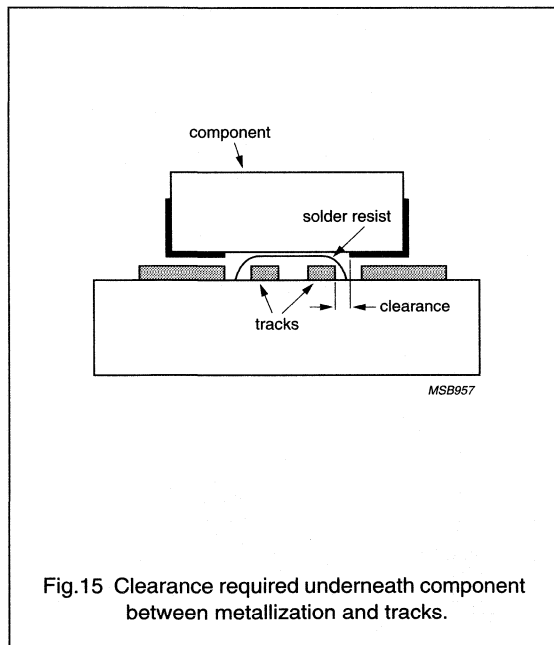


Fig.15 Clearance required underneath component between metallization and tracks.

For components that need the additional clearance, the footprints on the following pages give the maximum space for tracks not connected to the solder lands (clearance  $\geq 0.1$  mm), for low-voltage applications. The number of tracks in this space is determined by the specified line resolution of the printed board.

### COMPONENT ORIENTATION DURING WAVE SOLDERING

Where applicable, footprints for wave soldering are given with the transport direction of the PCB. This is given as either a 'preferred transport direction during soldering' or 'transport direction during soldering'.

Components with small terminals and non-wettable bodies, have a smaller risk of dry joints, especially when using carrierless soldering as the components are placed according to the 'preferred orientation'.

Components have no orientation preference for reflow soldering.

### RECOMMENDED FOOTPRINTS

The recommended footprints for our discrete semiconductor packages are given on the following pages. For their dimensional outline drawings, refer to Chapter 2: Package outlines.

# Soldering guidelines and SMD footprint design

## Chapter 4

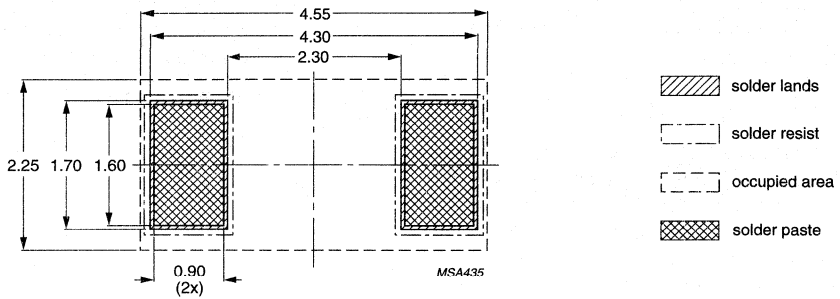


Fig.16 Reflow soldering footprint for SOD80(C).

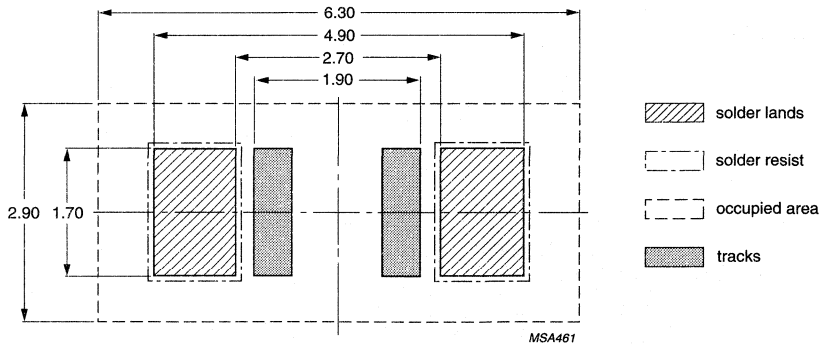


Fig.17 Wave soldering footprint for SOD80(C).



Soldering guidelines and SMD footprint design

Chapter 4

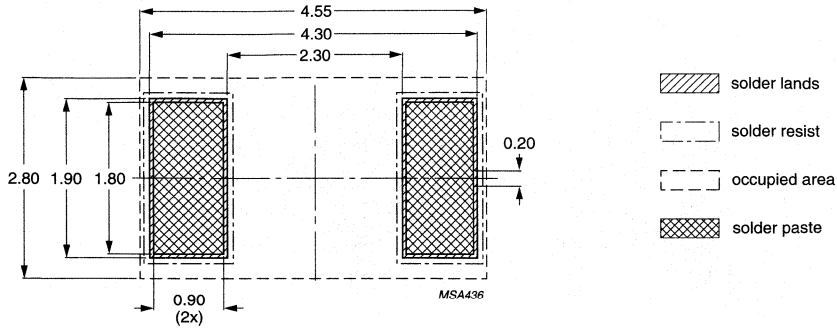


Fig.18 Reflow soldering footprint for SOD87.

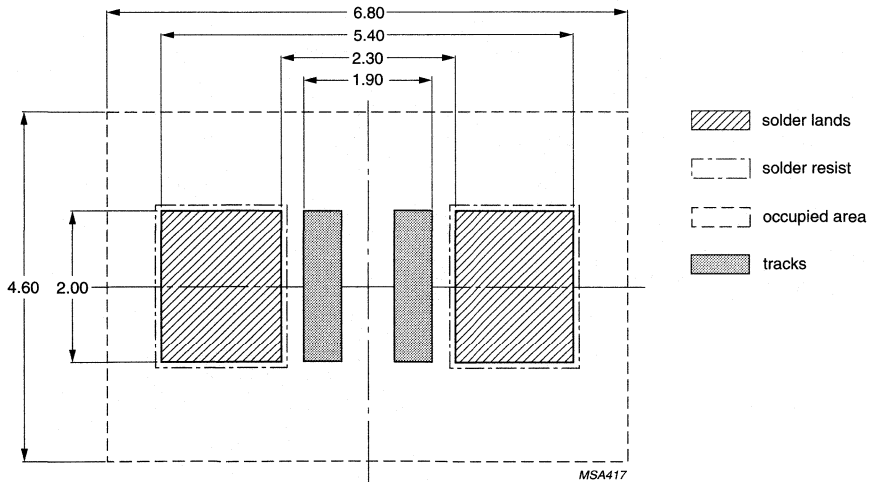


Fig.19 Wave soldering footprint for SOD87.

Soldering guidelines and SMD footprint design

Chapter 4

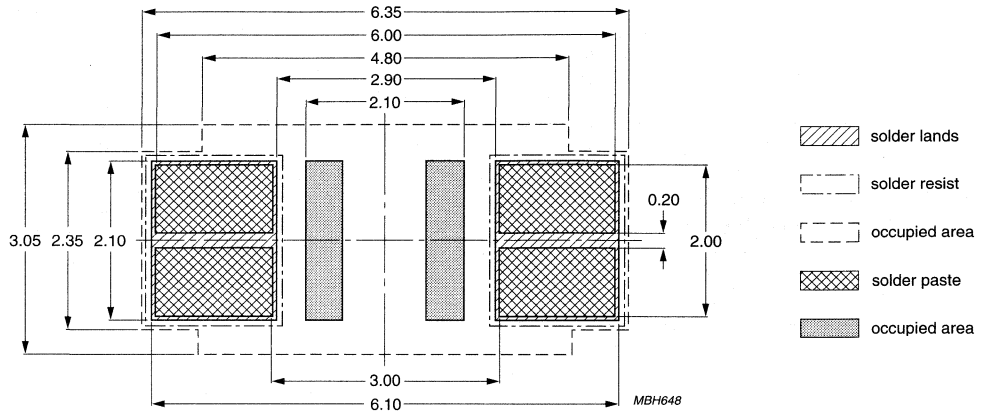


Fig.20 Reflow soldering footprint for SOD106.

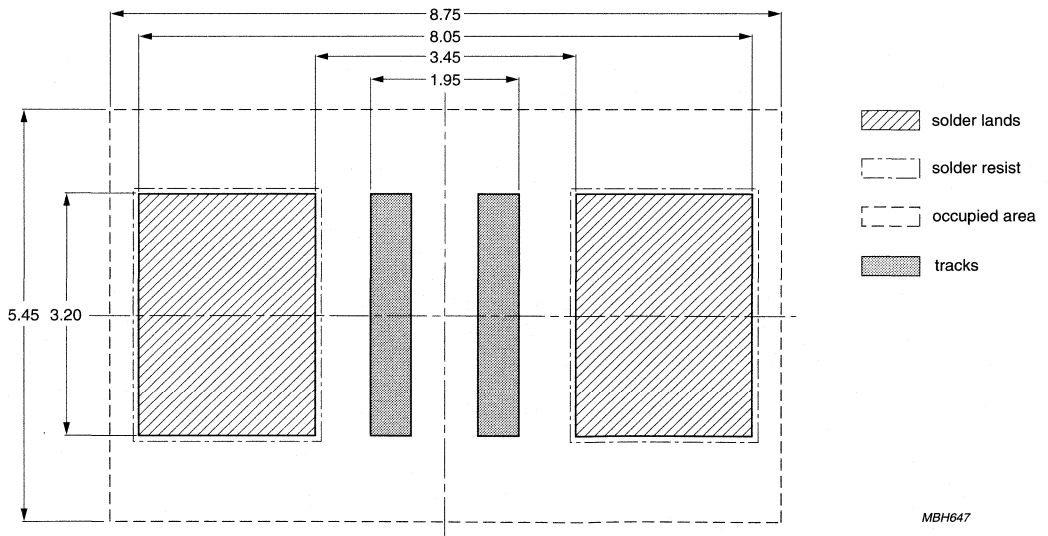


Fig.21 Wave soldering footprint for SOD106.

Soldering guidelines and SMD footprint design

Chapter 4

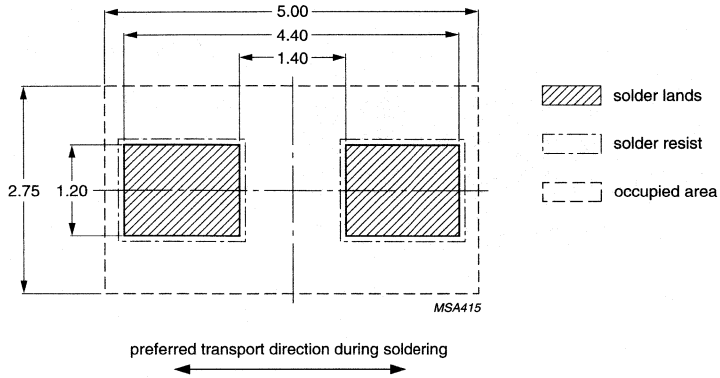


Fig.22 Reflow soldering footprint for SOD106(A).

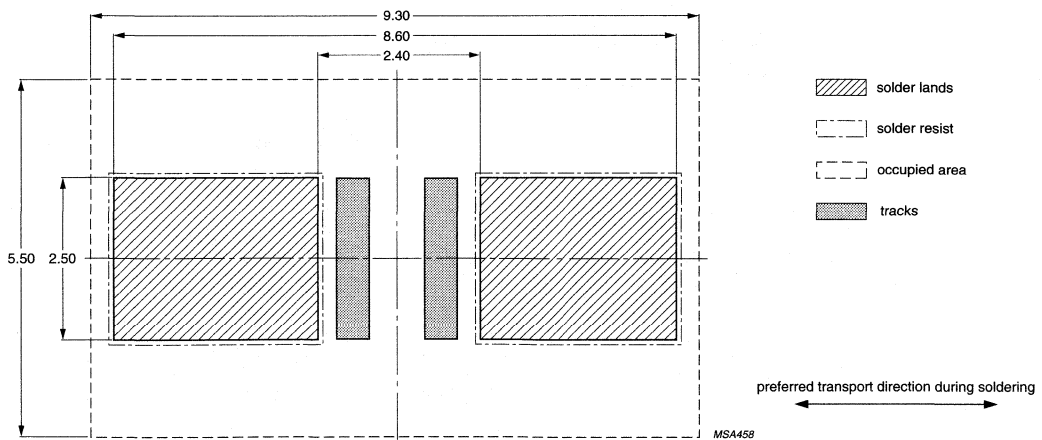


Fig.23 Wave soldering footprint for SOD106(A).

# Soldering guidelines and SMD footprint design

## Chapter 4

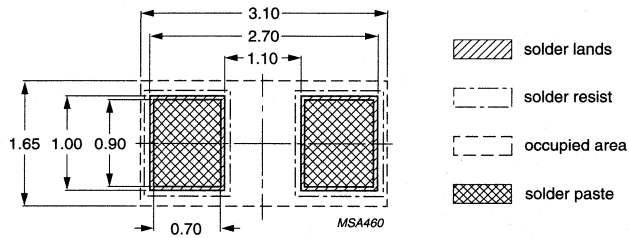


Fig.24 Reflow soldering footprint for SOD110.

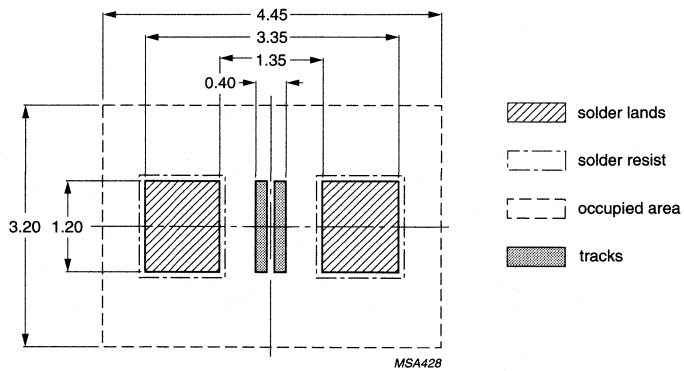


Fig.25 Wave soldering footprint for SOD110.

Soldering guidelines and SMD  
footprint design

Chapter 4

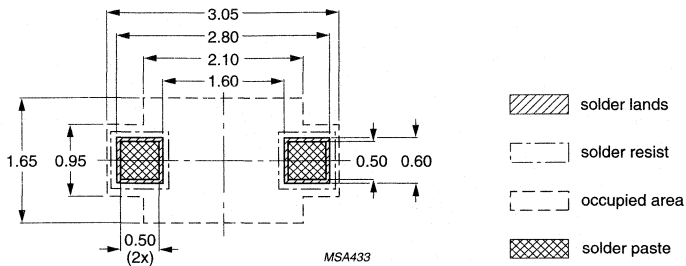


Fig.26 Reflow soldering footprint for SOD323 (SC-76).

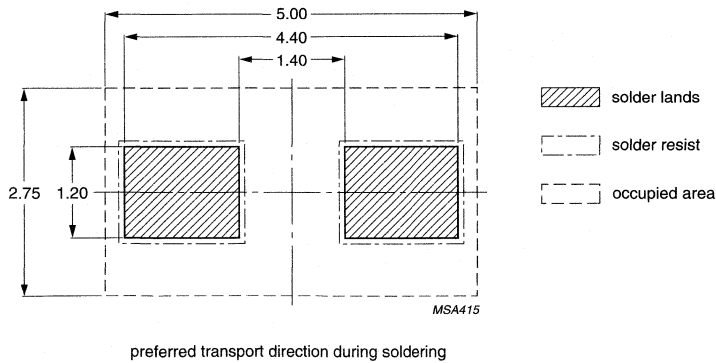


Fig.27 Wave soldering footprint for SOD323 (SC-76).

# Soldering guidelines and SMD footprint design

## Chapter 4

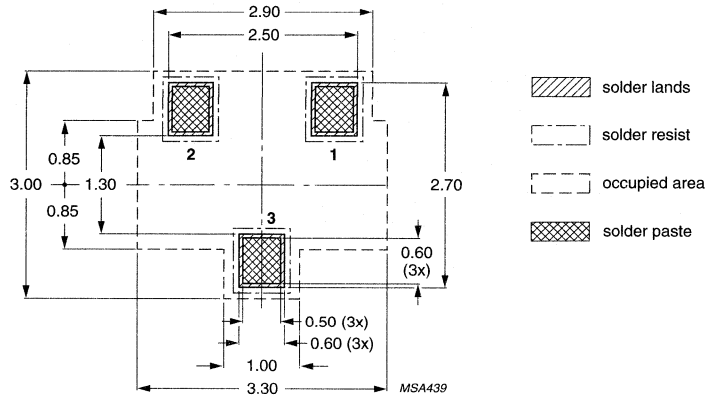


Fig.28 Reflow soldering footprint for SOT23.

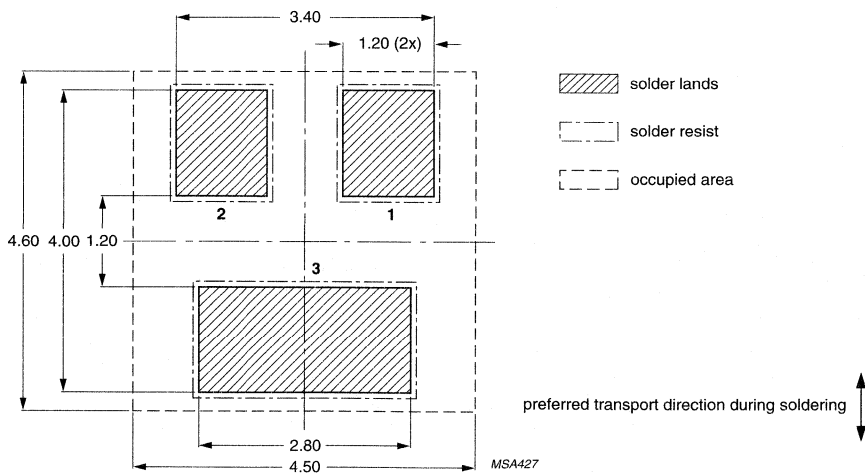


Fig.29 Wave soldering footprint for SOT23.

Soldering guidelines and SMD footprint design

Chapter 4

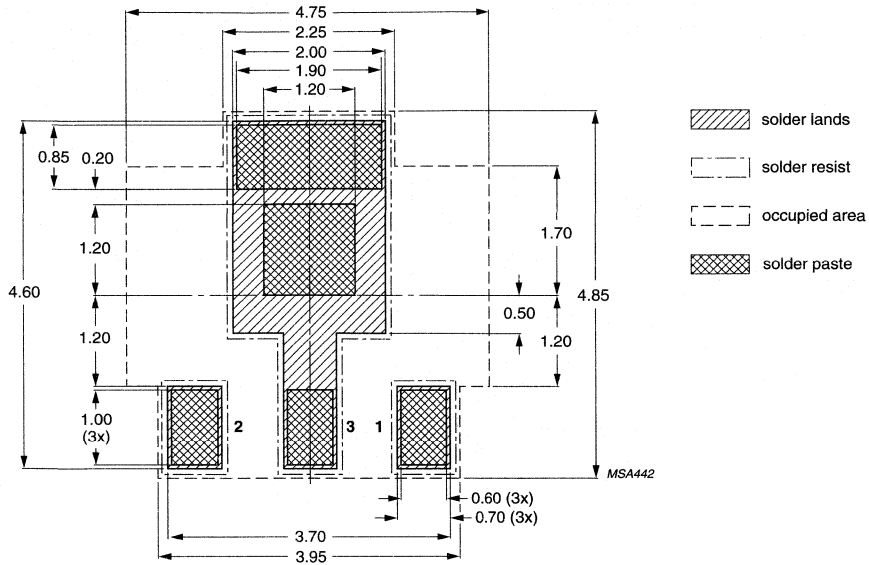
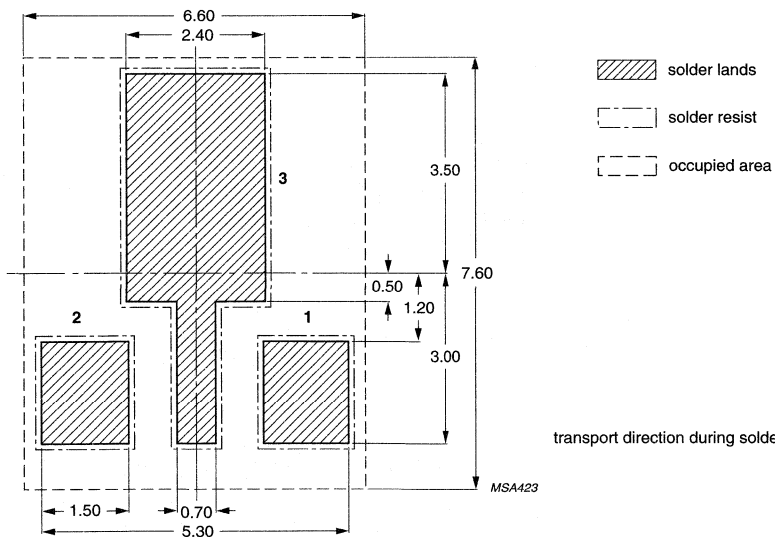


Fig.30 Reflow soldering footprint for SOT89 (SC-62).



Not recommended for wave soldering (see Fig.7).

Fig.31 Wave soldering footprint for SOT89 (SC-62).

# Soldering guidelines and SMD footprint design

## Chapter 4

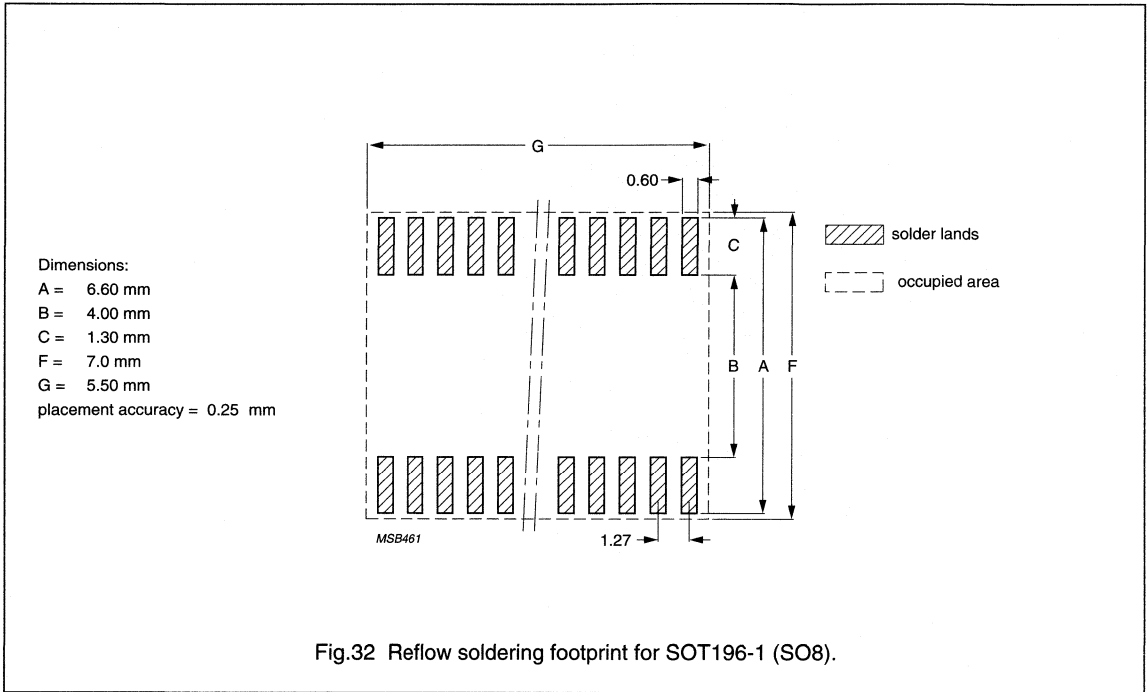


Fig.32 Reflow soldering footprint for SOT196-1 (SO8).

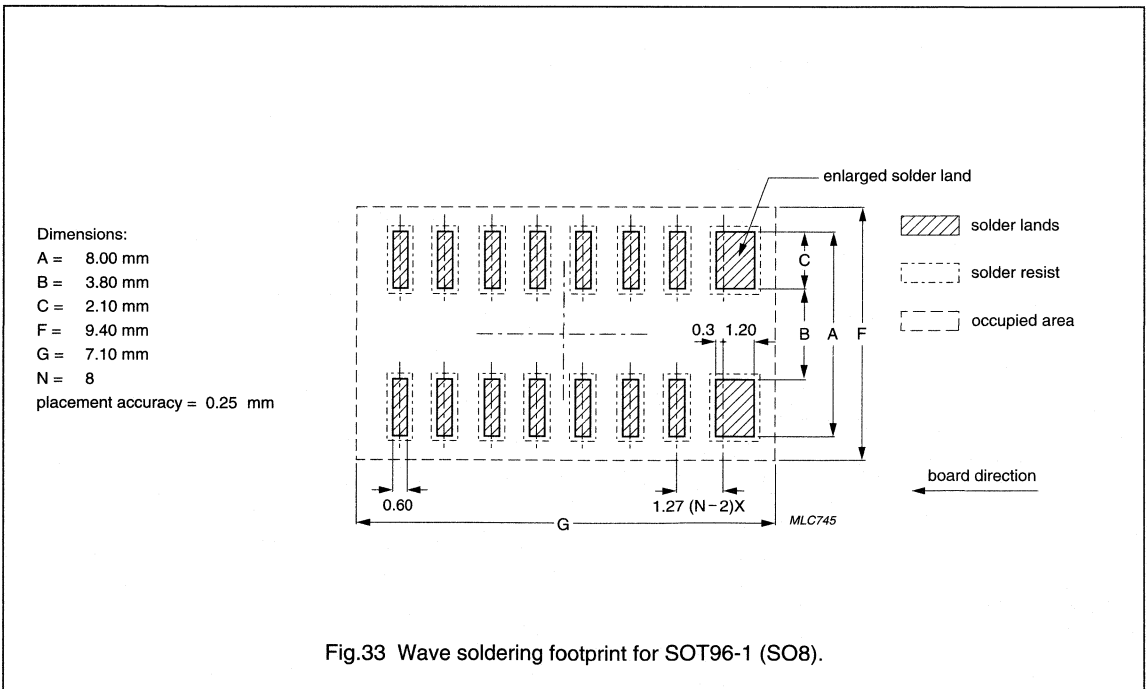


Fig.33 Wave soldering footprint for SOT96-1 (SO8).



# Soldering guidelines and SMD footprint design

## Chapter 4

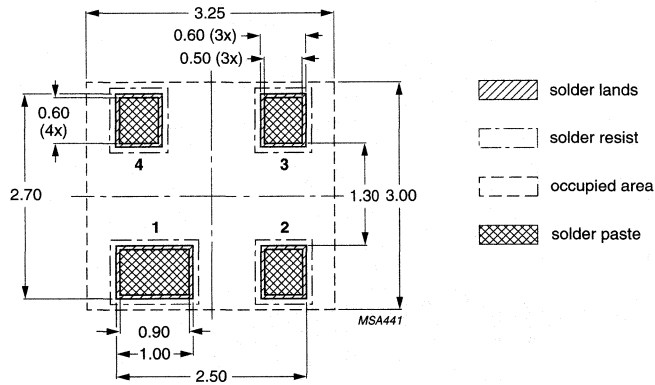


Fig.34 Reflow soldering footprint for SOT143 (footprint for SOT143R is mirror image).

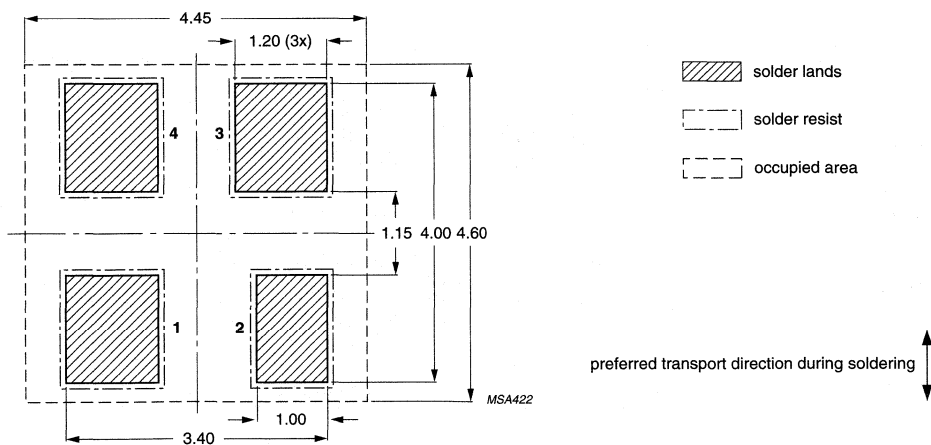


Fig.35 Wave soldering footprint for SOT143 (footprint for SOT143R is mirror image).

# Soldering guidelines and SMD footprint design

## Chapter 4

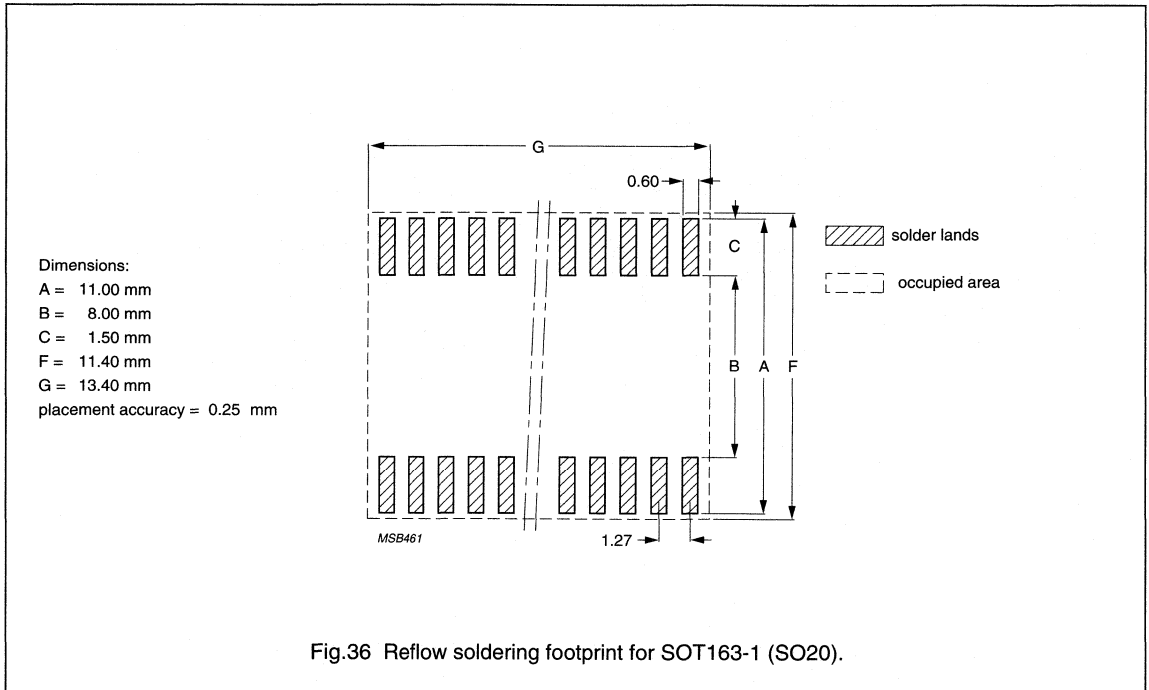


Fig.36 Reflow soldering footprint for SOT163-1 (SO20).

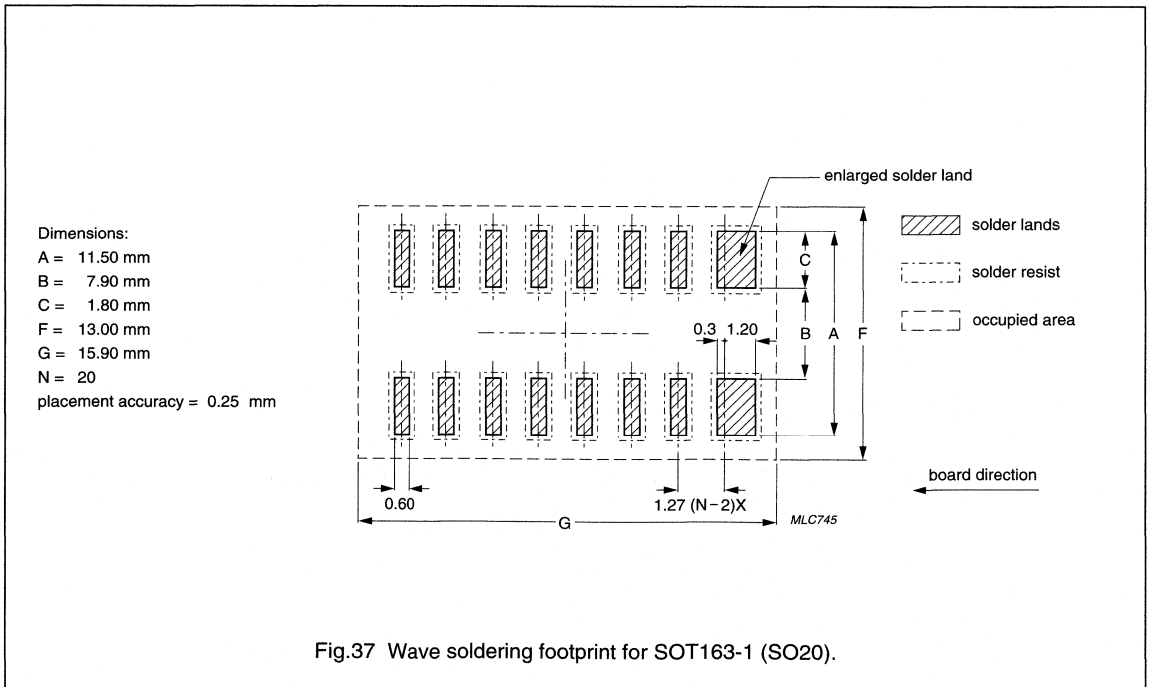


Fig.37 Wave soldering footprint for SOT163-1 (SO20).

Soldering guidelines and SMD footprint design

Chapter 4

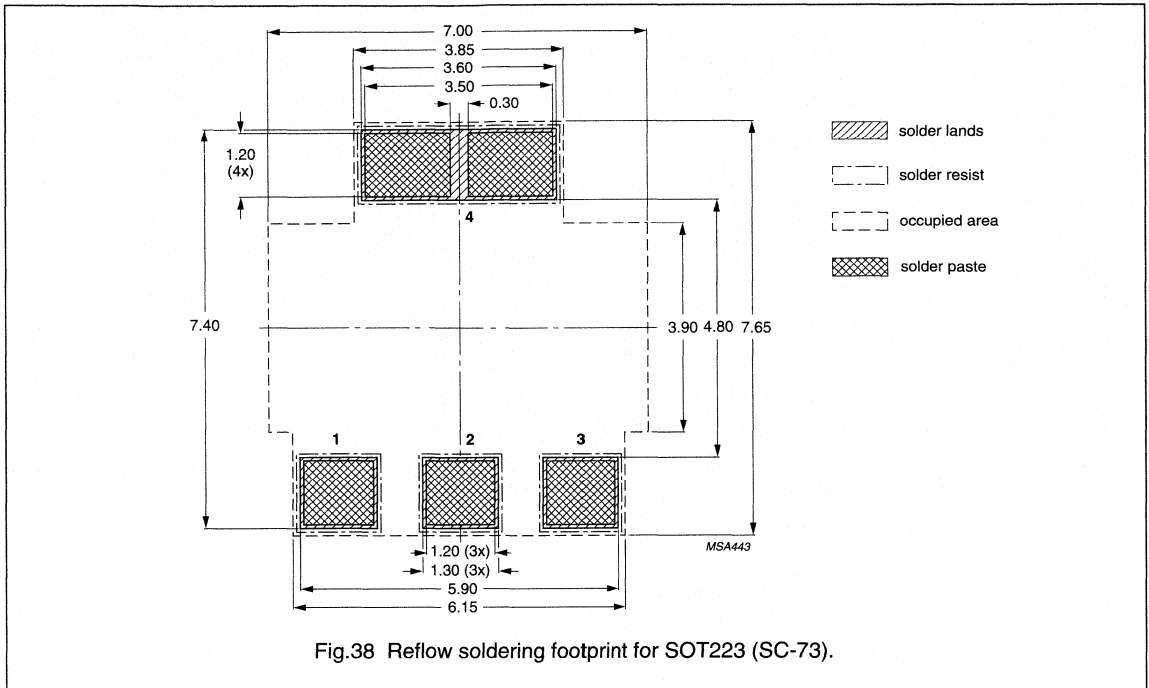


Fig.38 Reflow soldering footprint for SOT223 (SC-73).

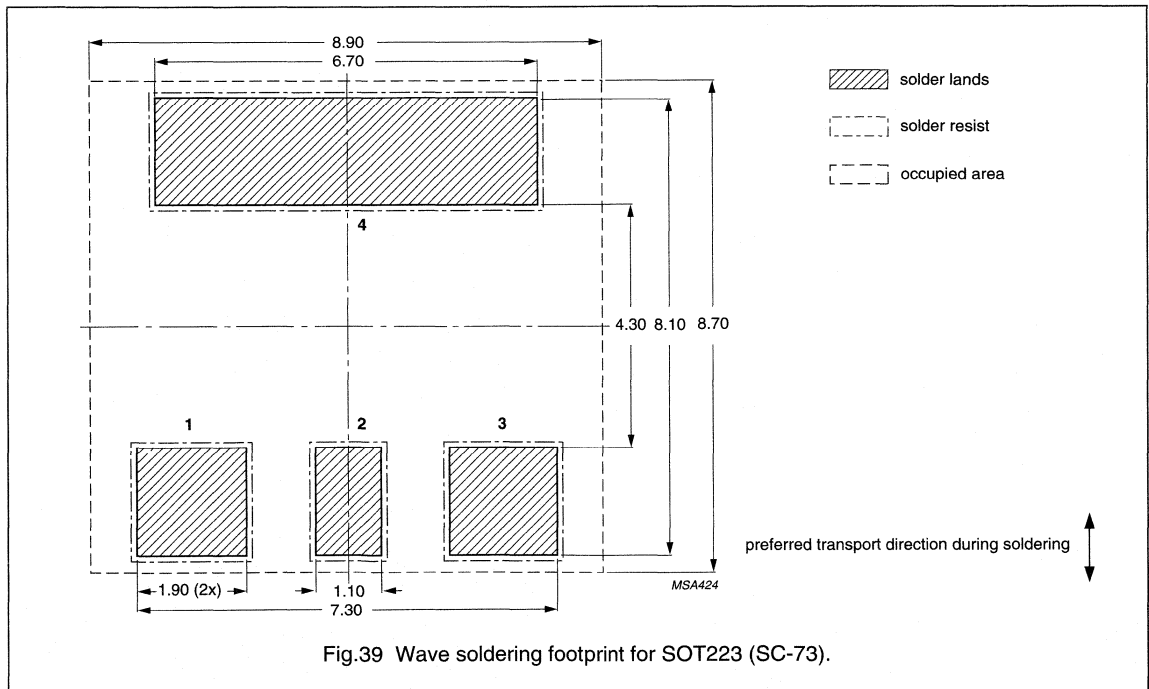


Fig.39 Wave soldering footprint for SOT223 (SC-73).

# Soldering guidelines and SMD footprint design

## Chapter 4

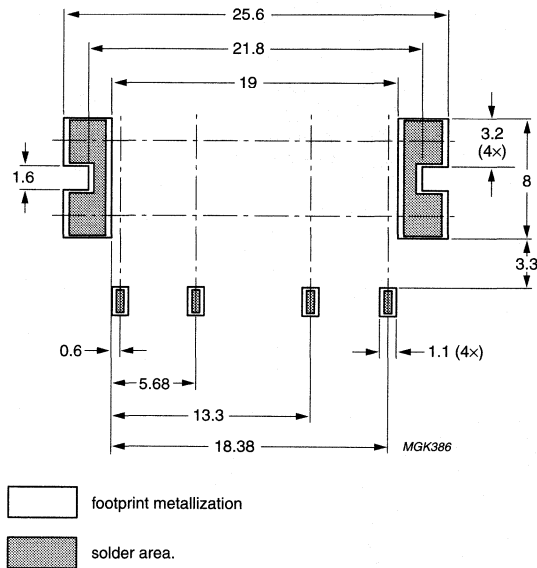


Fig.40 Reflow soldering footprint for SOT321 (not suitable for wave soldering).

# Soldering guidelines and SMD footprint design

## Chapter 4

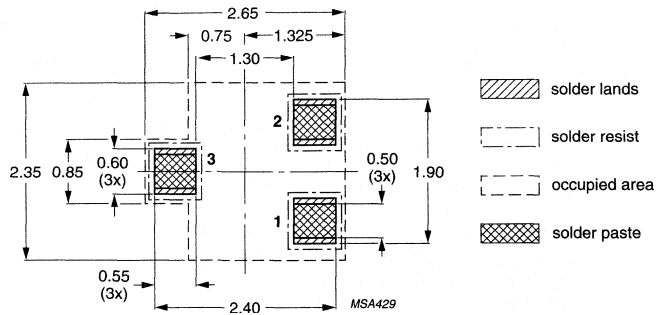


Fig.41 Reflow soldering footprint for SOT323 (SC-70).

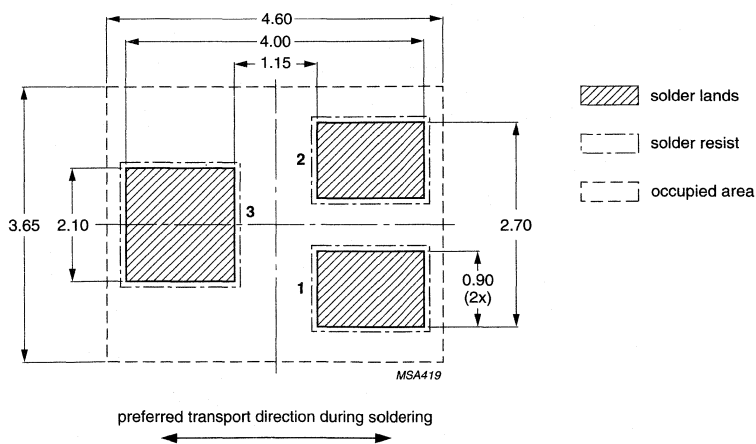


Fig.42 Wave soldering footprint for SOT323 (SC-70).

# Soldering guidelines and SMD footprint design

## Chapter 4

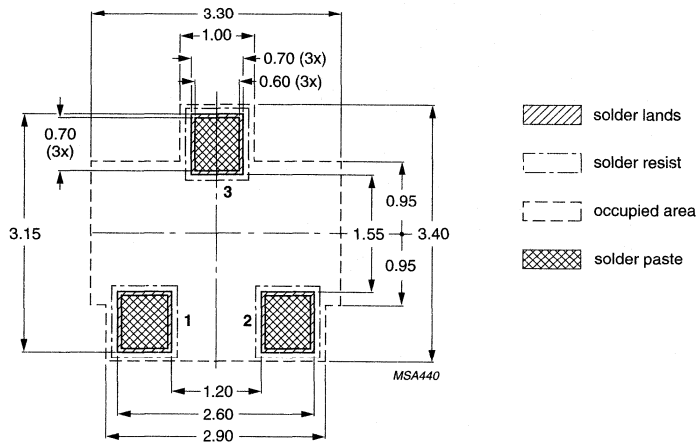


Fig.43 Reflow soldering footprint for SOT346 (SC-59).

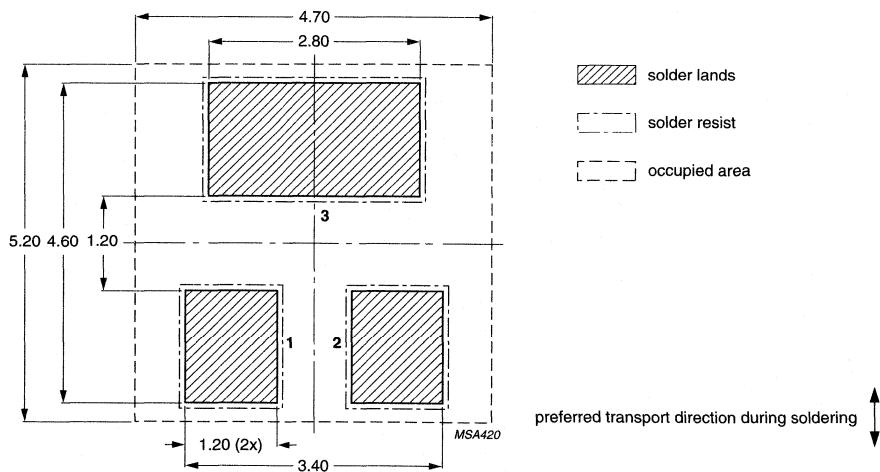


Fig.44 Wave soldering footprint for SOT346 (SC-59).

Soldering guidelines and SMD footprint design

Chapter 4

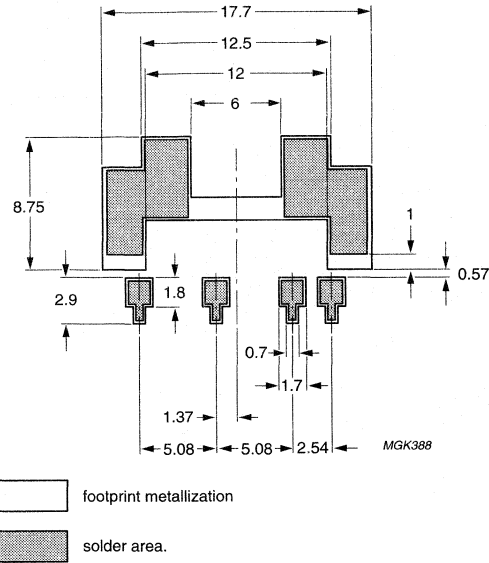


Fig.45 Reflow soldering footprint for SOT388 (not suitable for wave soldering).

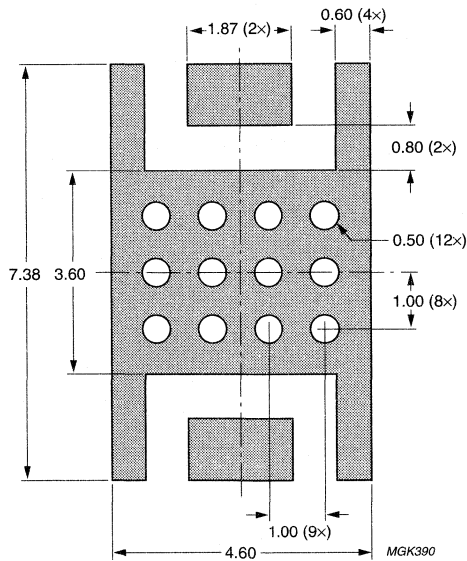


Fig.46 Reflow soldering footprint for SOT409 (not suitable for wave soldering).

# Soldering guidelines and SMD footprint design

## Chapter 4

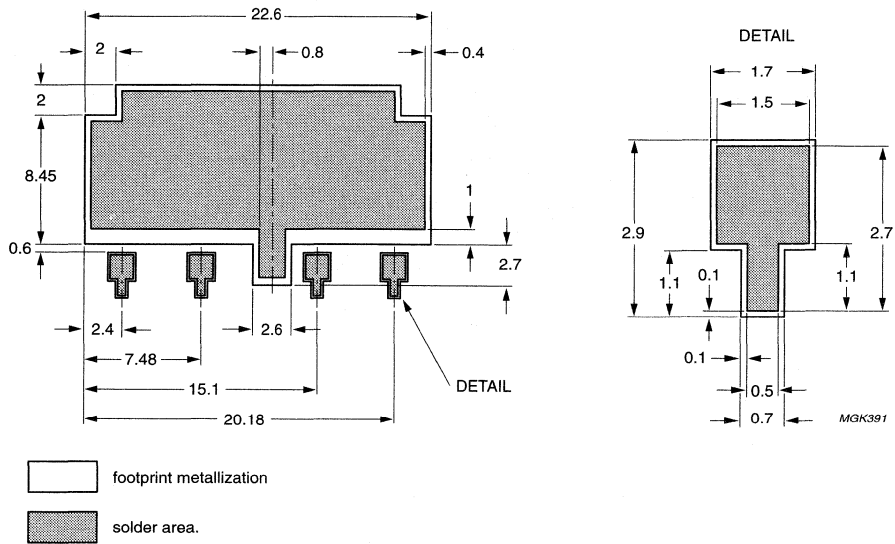


Fig.47 Reflow soldering footprint for SOT421 (not suitable for wave soldering).



Soldering guidelines and SMD footprint design

Chapter 4

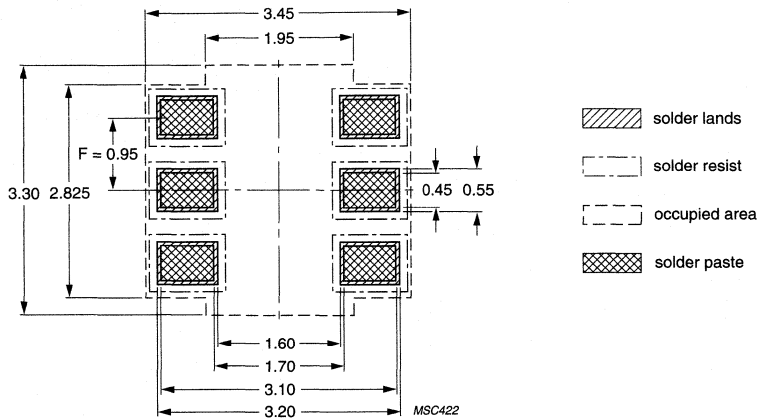


Fig.48 Reflow soldering footprint for SOT457 (SC-74).

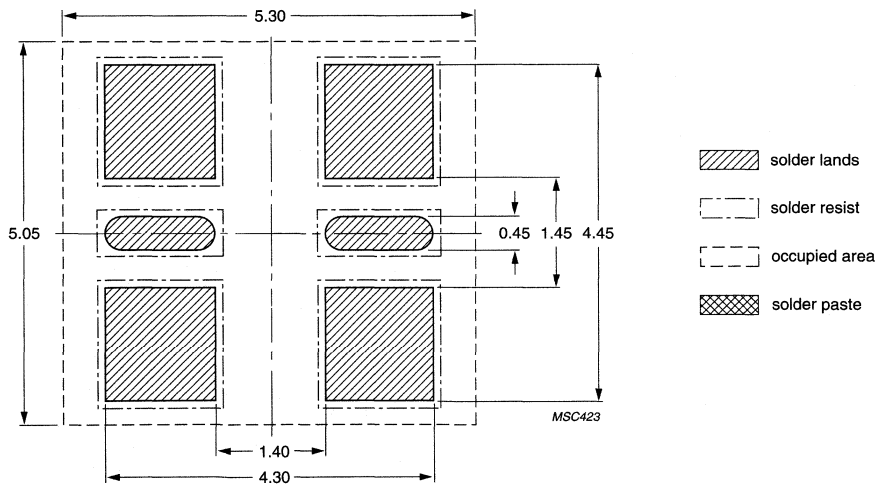


Fig.49 Wave soldering footprint for SOT457 (SC-74).



# Thermal considerations

# Chapter 5

## INTRODUCTION

The perfect power switch is not yet available. All power semiconductors dissipate power internally both during the on-state and during the transition between the on and off states. The amount of power dissipated internally generally speaking increases in line with the power being switched by the semiconductor. The capability of a switch to operate in a particular circuit will therefore depend upon the amount of power dissipated internally and the rise in the operating temperature of the silicon junction that this power dissipation causes. It is therefore important that circuit designers are familiar with the thermal characteristics of power semiconductors and are able to calculate power dissipation limits and junction operating temperatures.

This chapter is divided into three parts. Part One describes the essential thermal properties of semiconductors and explains the concept of a limit, in terms of continuous mode and pulse mode operation. Part Two gives worked examples showing junction temperature calculations for a variety of applied power pulse waveforms. Part Three discusses component heat dissipation and heatsink design.

## PART ONE: THERMAL PROPERTIES

### The power dissipation limit

The maximum allowable power dissipation forms a limit to the safe operating area of power transistors. Power dissipation causes a rise in junction temperature which will, in turn, start chemical and metallurgical changes. The rate at which these changes proceed is exponentially related to temperature, and thus prolonged operation of a power transistor above its junction temperature rating is liable to result in reduced life. Operation of a device at, or below, its power dissipation rating (together with careful consideration of thermal resistances associated with the device) ensures that the junction temperature rating is not exceeded.

All power semiconductors have a power dissipation limitation. For rectifier products such as diodes, thyristors and triacs, the power dissipation rating can be easily translated in terms of current ratings; in the on-state the voltage drop is well defined. Transistors are, however, somewhat more complicated. A transistor, be it a power MOSFET or a bipolar, can operate in its on-state at any voltage up to its maximum rating depending on the circuit conditions. It is therefore necessary to specify a Safe Operating Area (SOA) for transistors which specifies the power dissipation limit in terms of a series of boundaries in

the current and voltage plane. These operating areas are usually presented for mounting base temperatures of 25 °C. At higher temperatures, operating conditions must be checked to ensure that junction temperatures are not exceeding the desired operating level.

### Continuous power dissipation

The total power dissipation in a semiconductor may be calculated from the product of the on-state voltage and the forward conduction current. The heat dissipated in the junction of the device flows through the thermal resistance between the junction and the mounting base,  $R_{thj-mb}$ . The thermal equivalent circuit of Fig.1 illustrates this heat flow;  $P_{tot}$  can be regarded as a thermal current, and the temperature difference between the junction and mounting base  $\Delta T_{j-mb}$  as a thermal voltage. By analogy with Ohm's law, it follows that:

$$P_{tot} = \frac{T_j - T_{mb}}{R_{thj-mb}} \tag{1}$$

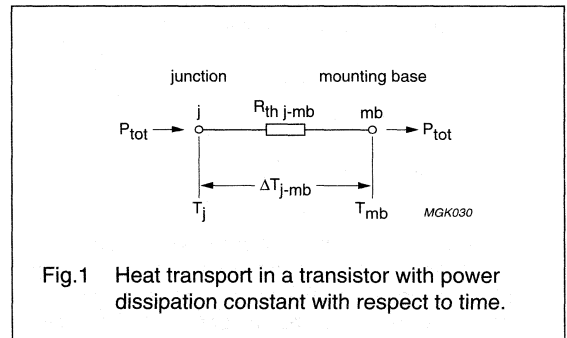


Fig.1 Heat transport in a transistor with power dissipation constant with respect to time.

Figure 2 shows the dependence of the maximum power dissipation on the temperature of the mounting base.  $P_{totmax}$  is limited either by a maximum temperature difference:

$$\Delta T_{j-mbmax} = T_{jmax} - T_{mbK} \tag{2}$$

or by the maximum junction temperature  $T_{jmax}$  ( $T_{mbK}$  is usually 25 °C and is the value of  $T_{mb}$  above which the maximum power dissipation must be reduced to maintain the operating point within the safe operating area).

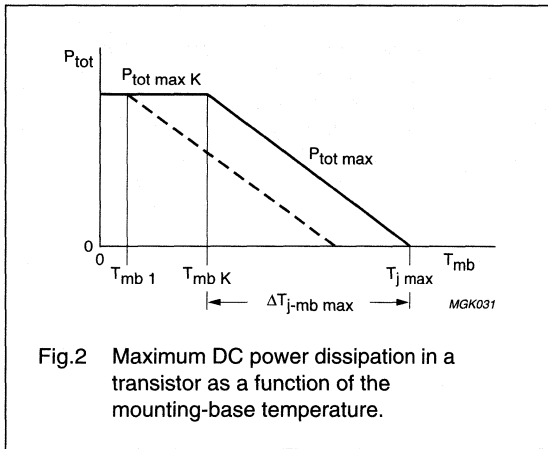
In the first case,  $T_{mb} \leq T_{mbK}$ :

$$P_{totmaxK} = \frac{\Delta T_{j-mbmax}}{R_{thj-mb}} \tag{3}$$

Thermal considerations

Chapter 5

that is, the power dissipation has a fixed limit value ( $P_{tot\ max\ K}$  is the maximum DC power dissipation below  $T_{mb\ K}$ ). If the transistor is subjected to a mounting-base temperature  $T_{mb\ 1}$ , its junction temperature will be less than  $T_{j\ max}$  by an amount ( $T_{mb\ K} - T_{mb\ 1}$ ), as shown by the broken line in Fig.2.



In the second case,  $T_{mb} > T_{mb\ K}$ :

$$P_{tot\ max} = \frac{T_{j\ max} - T_{mb}}{R_{thj-mb}} \tag{4}$$

that is, the power dissipation must be reduced as the mounting base temperature increases along the sloping straight line in Fig.2. Equation (4) shows that the lower the thermal resistance  $R_{thj-mb}$ , the steeper is the slope of the line. In this case,  $T_{mb}$  is the maximum mounting-base temperature that can occur in operation.

**Example**

The following data is provided for a particular transistor.

$$P_{tot\ max\ K} = 75\ W$$

$$T_{j\ max} = 175\ ^\circ C$$

$$R_{thj-mb} \leq 2\ K/W$$

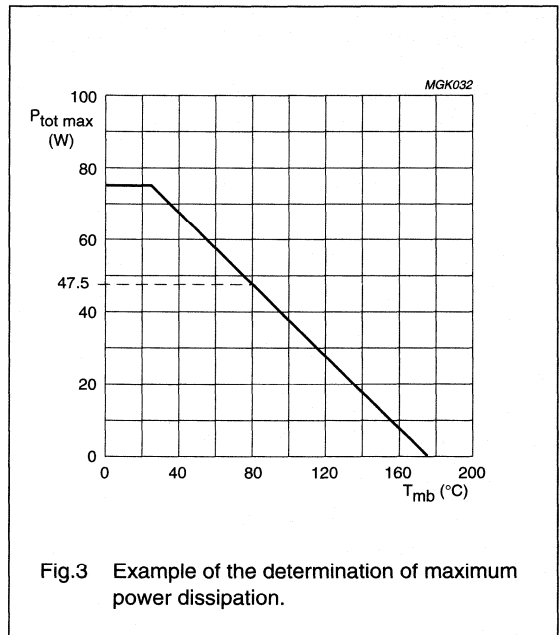
The maximum permissible power dissipation for continuous operation at a maximum mounting-base temperature of  $T_{mb} = 80\ ^\circ C$  is required.

Note that the maximum value of  $T_{mb}$  is chosen to be significantly higher than the maximum ambient temperature to prevent an excessively large heatsink being required.

From Equation (4) we obtain:

$$P_{tot\ max} = \frac{175 - 80}{2}\ W = 47.5\ W$$

Provided that the transistor is operated within SOA limits, this value is permissible since it is below  $P_{tot\ max\ K}$ . The same result can be obtained graphically from the  $P_{tot\ max}$  diagram (Fig.3) for the relevant transistor.



**Pulse power operation**

When a power transistor is subjected to a pulsed load, higher peak power dissipation is permitted. The materials in a power transistor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device. The power dissipation limit may be extended for intermittent operation. The size of the extension will depend on the duration of the operation period (that is, pulse duration) and the frequency with which operation occurs (that is, duty factor).

## Thermal considerations

## Chapter 5

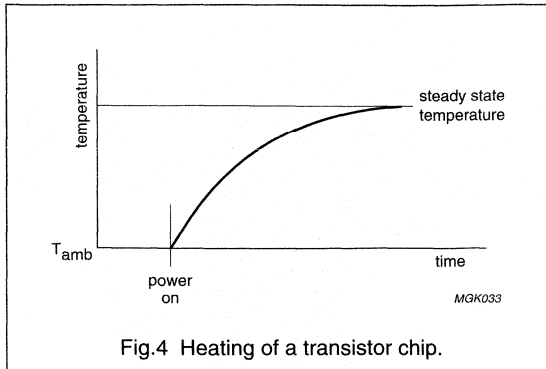


Fig.4 Heating of a transistor chip.

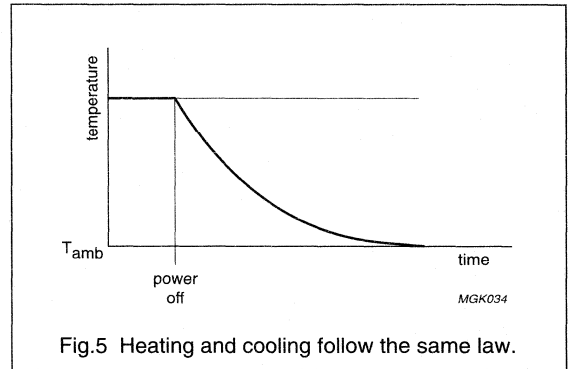


Fig.5 Heating and cooling follow the same law.

If power is applied to a transistor, the device will immediately start to warm up (see Fig.4). If the power dissipation continues, a balance will be struck between heat generation and removal resulting in the stabilization of  $T_j$  and  $\Delta T_{j-mb}$ . Some heat energy will be stored by the thermal capacity of the device, and the stable conditions will be determined by the thermal resistances associated with the transistor and its thermal environment. When the power dissipation ceases, the device will cool (the heating and cooling laws will be identical, see Fig.5). However, if the power dissipation ceases before the temperature of the transistor stabilizes, the peak values of  $T_j$  and  $\Delta T_{j-mb}$  will be less than the values reached for the same level of continuous power dissipation (see Fig.6). If the second pulse is identical to the first, the peak temperature attained by the device at the end of the second pulse will be greater than that at the end of the first pulse. Further pulses will build up the temperature until some new stable situation is attained (see Fig.7). The temperature of the device in this stable condition will fluctuate above and below the mean. If the upward excursions extend into the region of excessive  $T_j$  then the life expectancy of the device may be reduced. This can happen with high-power low-duty-factor pulses, even though the average power is below the DC rating of the device.

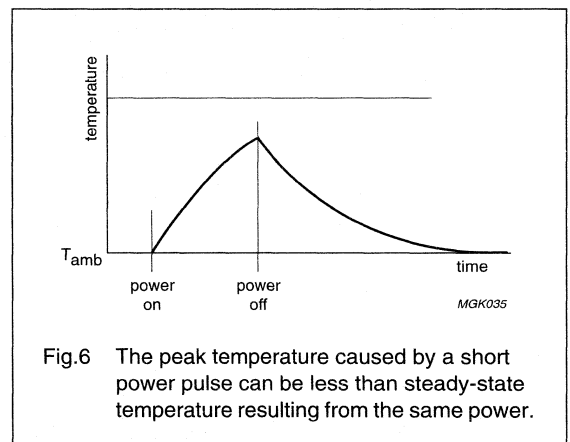


Fig.6 The peak temperature caused by a short power pulse can be less than steady-state temperature resulting from the same power.

Figure 8 shows a typical safe operating area for DC operation of a power MOSFET. The corresponding rectangular-pulse operating areas with a fixed duty factor,  $\delta = 0$ , and the pulse time  $t_p$  as a parameter, are also shown. These boundaries represent the largest possible extension of the operating area for particular pulse times. When the pulse time becomes very short, the power dissipation does not have a limiting action and the pulse current and maximum voltage form the only limits. This rectangle represents the largest possible pulse operating area.

Thermal considerations

Chapter 5

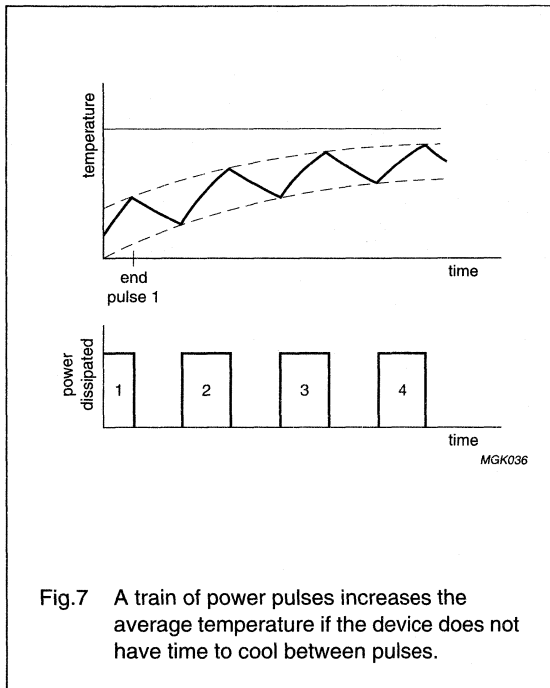


Fig.7 A train of power pulses increases the average temperature if the device does not have time to cool between pulses.

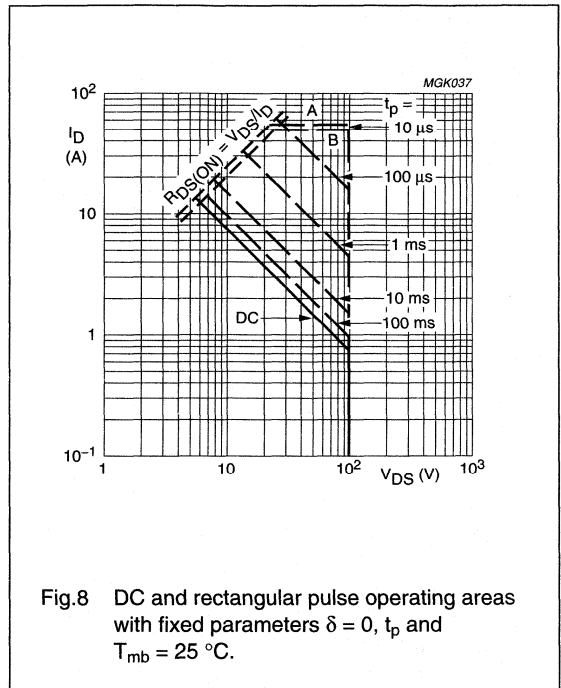


Fig.8 DC and rectangular pulse operating areas with fixed parameters  $\delta = 0$ ,  $t_p$  and  $T_{mb} = 25^\circ C$ .

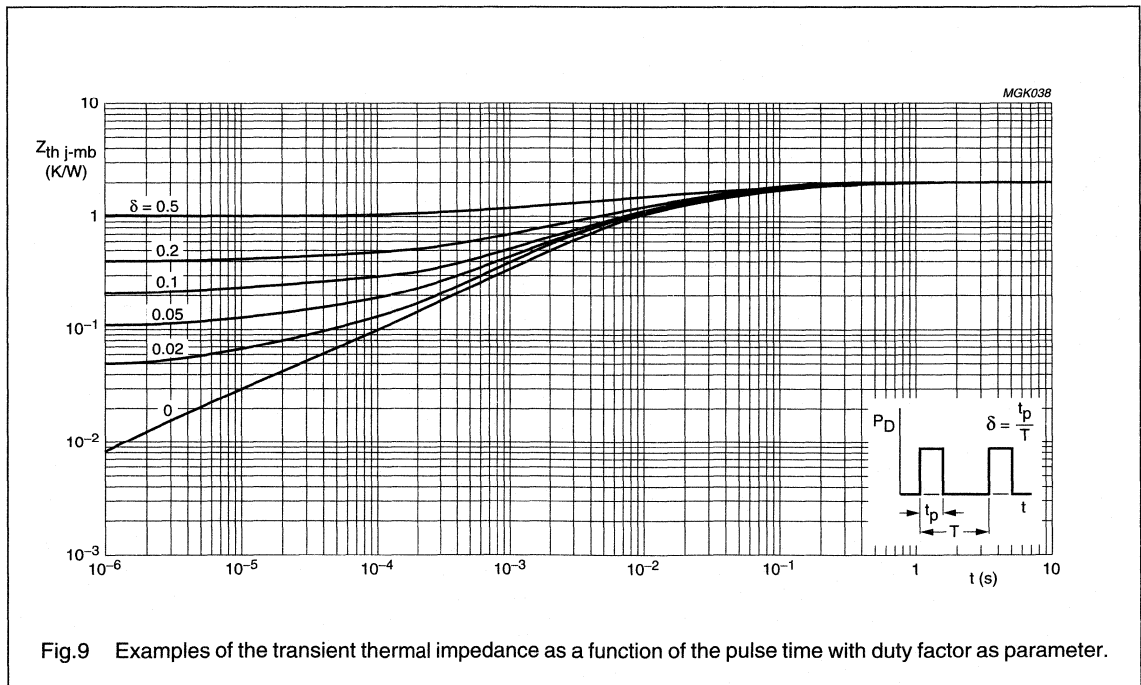


Fig.9 Examples of the transient thermal impedance as a function of the pulse time with duty factor as parameter.

# Thermal considerations

# Chapter 5

In general, the shorter the pulse and the lower the frequency, the lower the temperature that the junction reaches. By analogy with Equation (3), it follows that:

$$P_{\text{tot M}} = \frac{T_j - T_{\text{mb}}}{Z_{\text{thj-mb}}} \quad (5)$$

where  $Z_{\text{thj-mb}}$  is the transient thermal impedance between the junction and mounting base of the device. It depends on the pulse duration  $t_p$ , and the duty factor  $\delta$ , where:

$$\delta = \frac{t_p}{T} \quad (6)$$

and  $T$  is the pulse period. Figure 9 shows a typical family of curves for thermal impedance against pulse duration, with duty factor as a parameter.

Again, the maximum pulse power dissipation is limited either by the maximum temperature difference  $\Delta T_{\text{j-mb max}}$  (Equation (2)), or by the maximum junction temperature  $T_{\text{jmax}}$ , and so by analogy with Equations (3) and (4):

$$P_{\text{tot max K}} = \frac{\Delta T_{\text{j-mb max}}}{Z_{\text{thj-mb}}} \quad (7)$$

when  $T_{\text{mb}} \leq T_{\text{mb K}}$ , and:

$$P_{\text{tot M max}} = \frac{T_{\text{jmax}} - T_{\text{mb}}}{Z_{\text{thj-mb}}} \quad (8)$$

when  $T_{\text{mb}} > T_{\text{mb K}}$ . That is, below a mounting-base temperature of  $T_{\text{mb K}}$ , the maximum power dissipation has a fixed limit value; and above  $T_{\text{mb K}}$ , the power dissipation must be reduced linearly with increasing mounting-base temperature.

### Short pulse duration (Fig.10a)

As the pulse duration becomes very short, the fluctuations of junction temperature become negligible, owing to the internal thermal capacity of the transistor. Consequently, the only factor to be considered is the heating of the junction by the average power dissipation; that is:

$$P_{\text{tot (av)}} = \delta P_{\text{tot M}} \quad (9)$$

The transient thermal impedance becomes:

$$\lim_{t_p \rightarrow 0} Z_{\text{thj-mb}} = \delta R_{\text{thj-mb}} \quad (10)$$

The  $Z_{\text{thj-mb}}$  curves approach this value asymptotically as  $t_p$  decreases. Figure 9 shows that, for duty factors in the range 0.1 to 0.5, the limit values given by Equation (10) have virtually been reached at  $t_p = 10^{-6}$  s.

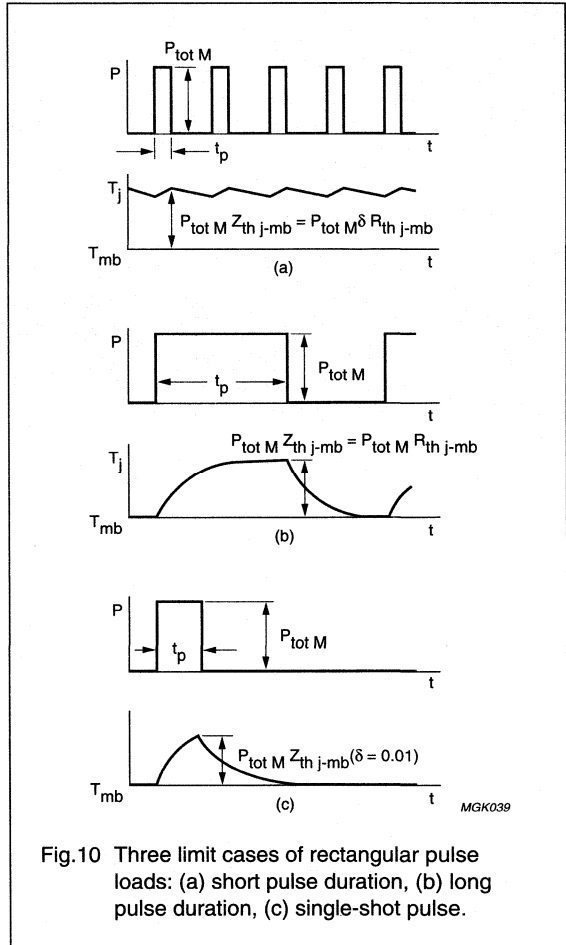


Fig.10 Three limit cases of rectangular pulse loads: (a) short pulse duration, (b) long pulse duration, (c) single-shot pulse.

### Long pulse duration (Fig.10b)

As the pulse duration increases, the junction temperature approaches a stationary value towards the end of a pulse. The transient thermal impedance tends to the thermal resistance for continuous power dissipation; that is:

$$\lim_{t_p \rightarrow \infty} Z_{\text{thj-mb}} = R_{\text{thj-mb}} \quad (11)$$

Figure 9 shows that  $Z_{\text{thj-mb}}$  approaches this value as  $t_p$  becomes large. In general, transient thermal effects die out in most power transistors within 0.1 to 1.0 seconds. This time depends on the material and construction of the case, the size of the chip, the way it is mounted, and other factors. Power pulses with a duration in excess of this time have approximately the same effect as a continuous load.

## Thermal considerations

## Chapter 5

**Single-short pulse (Fig.10c)**

As the duty factor becomes very small, the junction tends to cool down completely between pulses so that each pulse can be treated individually. When considering single pulses, the  $Z_{thj-mb}$  values for  $\delta = 0$  (Fig.9) give sufficiently accurate results.

**PART TWO: WORKED EXAMPLES****Calculating junction temperatures**

Most applications which include power semiconductors usually involve some form of pulse mode operation. This section gives several worked examples showing how junction temperatures can be simply calculated. Examples are given for a variety of waveforms:

1. periodic waveforms
2. single-shot waveforms
3. composite waveforms
4. a pulse burst
5. non-rectangular pulses.

From the point of view of reliability, it is most important to know what the peak junction temperature will be when the

power waveform is applied and also what the average junction temperature is going to be.

Peak junction temperature will usually occur at the end of an applied pulse and its calculation will involve transient thermal impedance. The average junction temperature (where applicable) is calculated by working out the average power dissipation using the DC thermal resistance.

When considering the junction temperature in a device, the following formula is used:

$$T_j = T_{mb} + \Delta T_{j-mb} \quad (12)$$

where  $\Delta T_{j-mb}$  is found from a rearrangement of Equation (7). In all the following examples the mounting base temperature ( $T_{mb}$ ) is assumed to be 75 °C.

**Periodic rectangular pulse**

Figure 11 shows an example of a periodic rectangular pulse. This type of pulse is commonly found in switching applications. 100 W is dissipated every 400  $\mu$ s for a period of 20  $\mu$ s, representing a duty cycle ( $\delta$ ) of 0.05.

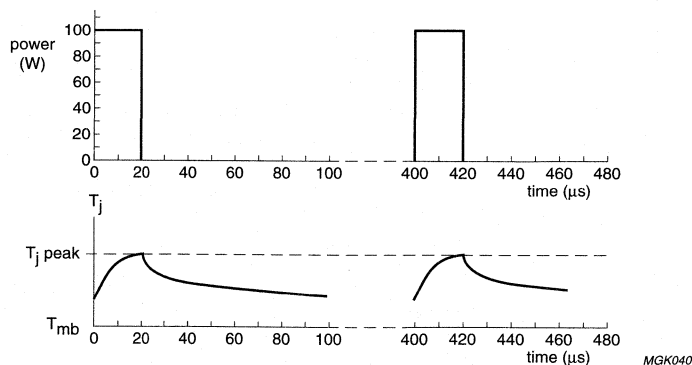


Fig.11 Periodic rectangular pulse.



# Thermal considerations

# Chapter 5

The peak junction temperature is calculated as follows:

**Peak  $T_j$ :**

$$t = 2 \times 10^{-5} \text{ s}$$

$$P = 100 \text{ W}$$

$$\delta = \frac{20}{100} = 0.05$$

$$Z_{thj-mb} = 0.12 \text{ K/W}$$

$$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.12 = 12 \text{ }^\circ\text{C}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 12 = 87 \text{ }^\circ\text{C}$$

**Average  $T_j$ :**

$$P_{av} = P \times \delta = 100 \times 0.05 = 5 \text{ W}$$

$$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 5 \times 2 = 10 \text{ }^\circ\text{C}$$

$$T_{j(av)} = T_{mb} + \Delta T_{j-mb(av)} = 75 + 10 = 85 \text{ }^\circ\text{C}$$

The value for  $Z_{thj-mb}$  is taken from the  $\delta = 0.05$  curve shown in Fig.12 (This diagram repeats Fig.9 but has been simplified for clarity). The above calculation shows that the peak junction temperature will be  $85 \text{ }^\circ\text{C}$ .

**Single shot rectangular pulse**

Figure 13 shows an example of a single shot rectangular pulse. The pulse used is the same as in the previous example, which should highlight the differences between periodic and single shot thermal calculations. For a single shot pulse, the time period between pulses is infinity, i.e. the duty cycle  $\delta = 0$ . In this example 100 W is dissipated for a period of  $20 \mu\text{s}$ . To work out the peak junction temperature the following steps are used:

$$t = 2 \times 10^{-5} \text{ s}$$

$$P = 100 \text{ W}$$

$$\delta = 0$$

$$Z_{thj-mb} = 0.04 \text{ K/W}$$

$$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.04 = 4 \text{ }^\circ\text{C}$$

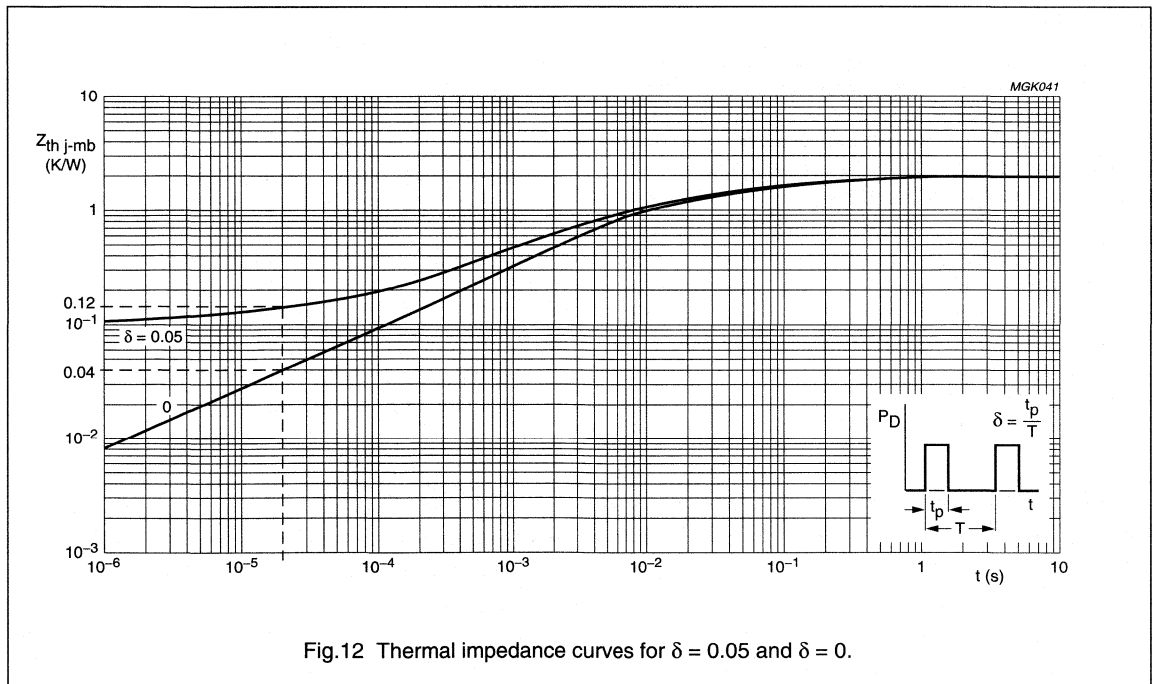


Fig.12 Thermal impedance curves for  $\delta = 0.05$  and  $\delta = 0$ .

# Thermal considerations

# Chapter 5

The value for  $Z_{th\ j-mb}$  is taken from the  $\delta = 0$  curve shown in Fig.12. The above calculation shows that the peak junction temperature will be 4 °C above the mounting base temperature.

For a single shot pulse, the average power dissipated and average junction temperature are not relevant.

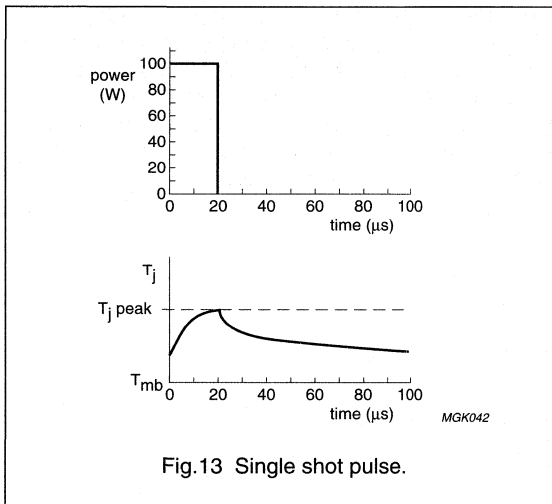


Fig.13 Single shot pulse.

### Composite rectangular pulse

In practice, a power device frequently has to handle composite waveforms, rather than the simple rectangular pulses shown so far. This type of signal can be simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of  $t_p$  and  $\delta$ .

By way of an example, consider the composite waveform shown in Fig.14. To show the way in which the method used for periodic rectangular pulses is extended to cover composite waveforms, the waveform shown has been chosen to be an extension of the periodic rectangular pulse example. The period is 400  $\mu s$ , and the waveform consists of three rectangular pulses, namely 40 W for 10  $\mu s$ , 20 W for 150  $\mu s$  and 100 W for 20  $\mu s$ . The peak junction temperature may be calculated at any point in the cycle. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time  $t_x$  in the first calculation and  $t_y$  in the second calculation. Positive pulses increase the junction temperature, while negative pulses decrease it.

### Calculation for time $t_x$

$$\begin{aligned} \Delta T_{j+mb@x} &= P_1 \times Z_{thj-mb}(t1) + P_2 \times Z_{thj-mb}(t3) \\ &+ P_3 \times Z_{thj-mb}(t4) - P_1 \times Z_{thj-mb}(t2) \\ &- P_2 \times Z_{thj-mb}(t4) \end{aligned} \quad (13)$$

In Equation (15), the values for  $P_1$ ,  $P_2$  and  $P_3$  are known:  $P_1 = 40$  W,  $P_2 = 20$  W and  $P_3 = 100$  W. The  $Z_{th}$  values are taken from Fig.9. For each term in the equation, the equivalent duty cycle must be worked out. For instance the first superimposed pulse in Fig.14 lasts for a time  $t_1 = 180 \mu s$ , representing a duty cycle of  $180/400 = 0.45 = \delta$ . These values can then be used in conjunction with Fig.9 to find a value for  $Z_{th}$ , which in this case is 0.9 K/W. Table 1 gives the values calculated for this example.

Table 1 Composite pulse parameters for time  $t_x$

		t1	t2	t3	t4
		180 $\mu s$	170 $\mu s$	150 $\mu s$	20 $\mu s$
Repetitive	$\delta$	0.450	0.425	0.375	0.050
T = 400 $\mu s$	$Z_{th}$	0.900	0.850	0.800	0.130
Single shot	$\delta$	0.000	0.000	0.000	0.000
T = $\infty$	$Z_{th}$	0.130	0.125	0.120	0.040

Substituting these values into Equation (15) for  $T_{j-mb@x}$  gives:

Repetitive:

$$\begin{aligned} \Delta T_{j-mb@x} &= 40 \times 0.9 + 20 \times 0.85 \\ &+ 100 \times 0.13 - 40 \times 0.85 - 20 \times 0.13 \\ &= 29.4 \text{ } ^\circ\text{C} \end{aligned}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 29.4 = 104.4 \text{ } ^\circ\text{C}$$

Single shot:

$$\begin{aligned} \Delta T_{j-mb@x} &= 40 \times 0.13 + 20 \times 0.125 \\ &+ 100 \times 0.04 - 40 \times 0.125 - 20 \times 0.04 \\ &= 5.9 \text{ } ^\circ\text{C} \end{aligned}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 5.9 = 80.9 \text{ } ^\circ\text{C}$$

Hence the peak values of  $T_j$  are 104.4 °C for the repetitive case, and 80.9 °C for the single shot case.

Thermal considerations

Chapter 5

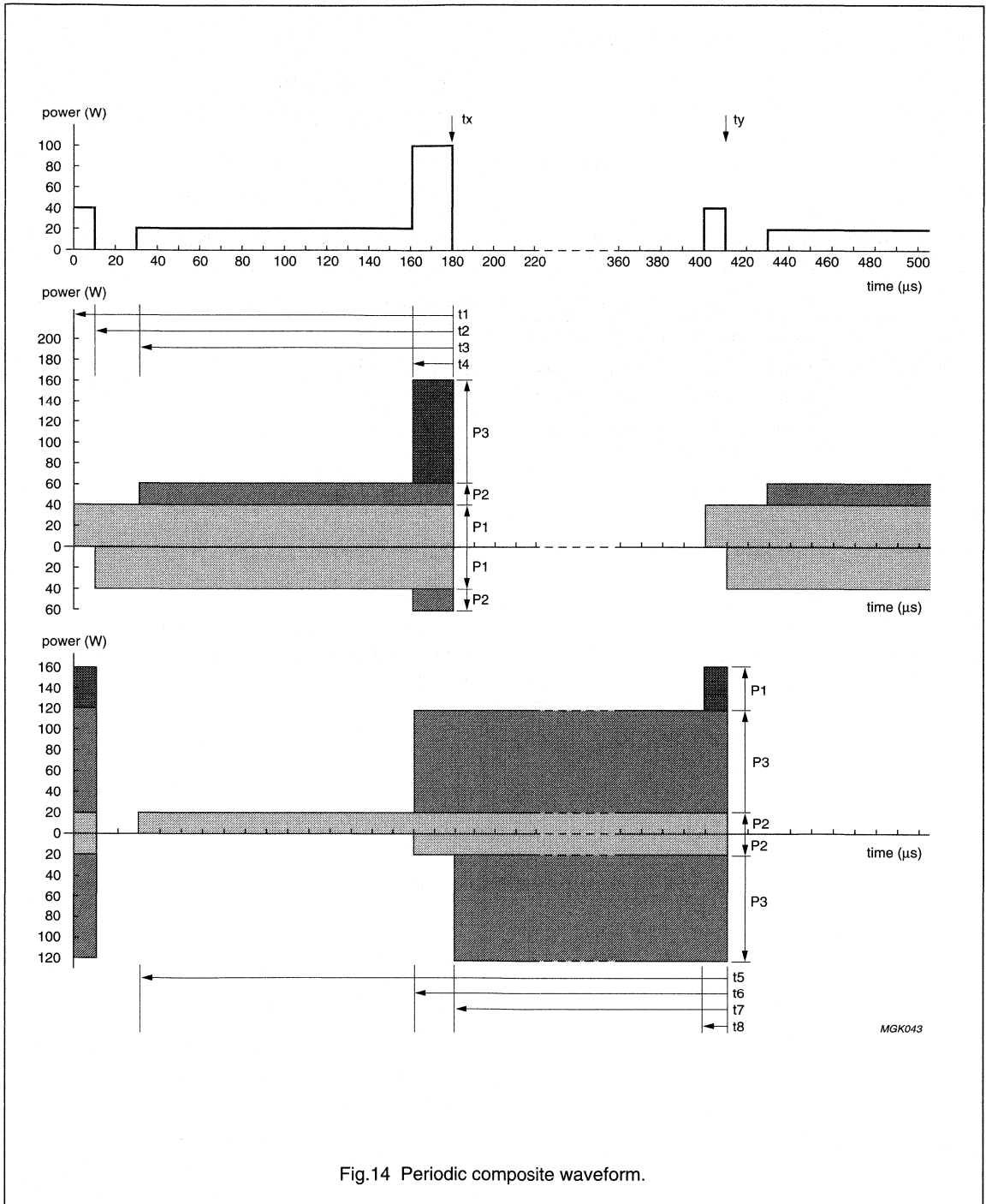


Fig.14 Periodic composite waveform.

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## Thermal considerations

## Chapter 5

**Calculation for time  $t_y$** 

$$\begin{aligned} \Delta T_{j+mb@y} &= P_2 \times Z_{thj-mb}(t5) + P_3 \times Z_{thj-mb}(t6) \\ &+ P_1 \times Z_{thj-mb}(t8) - P_2 \times Z_{thj-mb}(t6) \\ &- P_3 \times Z_{thj-mb}(t7) \end{aligned} \quad (14)$$

Where  $Z_{th-mb}(t)$  is the transient thermal impedance for a pulse time  $t$ .

**Table 2** Composite pulse parameters for time  $t_y$ 

		t5	t6	t7	t8
		380 $\mu$ s	250 $\mu$ s	230 $\mu$ s	10 $\mu$ s
Repetitive	$\delta$	0.950	0.625	0.575	0.025
$T = 400 \mu$ s	$Z_{th}$	1.950	1.300	1.250	0.080
Single shot	$\delta$	0.000	0.000	0.000	0.000
$T = \infty$	$Z_{th}$	0.200	0.160	0.150	0.030

Substituting these values into Equation (15) for  $T_{j-mb}(y)$  gives:

Repetitive:

$$\begin{aligned} \Delta T_{j-mb}(y) &= 20 \times 1.95 + 100 \times 1.3 \\ &+ 40 \times 0.08 - 20 \times 1.3 - 100 \times 1.25 \\ &= 21.2 \text{ }^\circ\text{C} \end{aligned}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 21.2 = 96.2 \text{ }^\circ\text{C}$$

Single shot:

$$\begin{aligned} \Delta T_{j-mb@y} &= 20 \times 0.2 + 100 \times 0.16 \\ &+ 40 \times 0.03 - 20 \times 0.16 - 100 \times 0.15 \\ &= 3 \text{ }^\circ\text{C} \end{aligned}$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 3 = 78 \text{ }^\circ\text{C}$$

Hence the peak values of  $T_j$  are 96.2  $^\circ\text{C}$  for the repetitive case, and 78  $^\circ\text{C}$  for the single shot case.

The average power dissipation and the average junction temperature can be calculated as follows:

$$\begin{aligned} P_{av} &= \frac{25 \times 10 + 5 \times 130 + 20 \times 100}{400} \\ &= 7.25 \text{ W} \end{aligned}$$

$$\begin{aligned} \Delta T_{j-mb(av)} &= P_{av} \times Z_{th-mb}(\delta = 1) \\ &= 7.25 \times 2 = 14.5 \text{ }^\circ\text{C} \end{aligned}$$

$$\begin{aligned} \Delta T_{j(av)} &= T_{mb} + \Delta T_{j-mb(av)} \\ &= 75 + 14.5 = 89.5 \text{ }^\circ\text{C} \end{aligned}$$

Clearly, the junction temperature at time  $t_x$  should be higher than that at time  $t_y$ , and this is proven in the above calculations.

# Thermal considerations

# Chapter 5

## Burst pulses

Power devices are frequently subjected to a burst of pulses. This type of signal can be treated as a composite waveform and as in the previous example simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of  $t_p$  and  $\delta$ .

Consider the waveform shown in Fig.15. The period is 240  $\mu$ s, and the burst consists of three rectangular pulses of 100 W power and 20 ms duration, separated by 30 ms. The peak junction temperature will occur at the end of each burst at time  $t = t_x = 140 \mu$ s. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time  $t_x$ . Positive pulses increase the junction temperature, while negative pulses decrease it.

$$\Delta T_{j+mb@x} = P \times Z_{thj-mb}(t1) + P \times Z_{thj-mb}(t3) + P \times Z_{thj-mb}(t5) - P \times Z_{thj-mb}(t2) - P \times Z_{thj-mb}(t4) \quad (15)$$

where  $Z_{thj-mb}(t)$  is the transient thermal impedance for a pulse time  $t$ .

The  $Z_{th}$  values are taken from Fig.9. For each term in the equation, the equivalent duty cycle must be worked out. These values can then be used in conjunction with Fig.9 to find a value for  $Z_{th}$ . Table 3 gives the values calculated for this example.

**Table 3** Burst Mode pulse parameters

		t1	t2	t3	t4	t5
		120 $\mu$ s	100 $\mu$ s	70 $\mu$ s	50 $\mu$ s	20 $\mu$ s
Repetitive	$\delta$	0.500	0.420	0.290	0.210	0.083
T = 240 $\mu$ s	$Z_{th}$	1.100	0.800	0.600	0.430	0.210
Single shot	$\delta$	0.000	0.000	0.000	0.000	0.000
T = $\infty$	$Z_{th}$	0.100	0.090	0.075	0.060	0.040

Substituting these values into Equation (17) gives:

Repetitive:

$$\Delta T_{j-mb@x} = 100 \times 1.10 + 100 \times 0.60 + 100 \times 0.21 - 100 \times 0.80 - 100 \times 0.43 = 68 \text{ } ^\circ\text{C}$$

$$T_j = 75 + 68 = 143 \text{ } ^\circ\text{C}$$

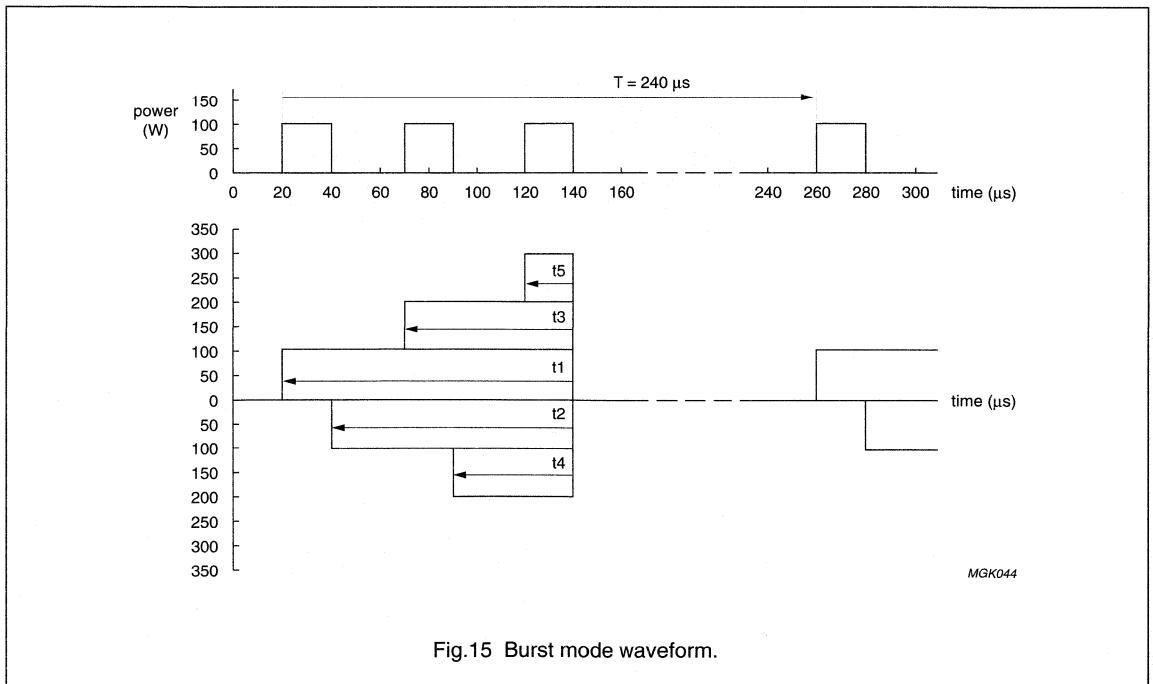


Fig.15 Burst mode waveform.

# Thermal considerations

# Chapter 5

Single Shot:

$$\begin{aligned} \Delta T_{j-mb@x} &= 100 \times 0.10 + 100 \times 0.075 \\ &+ 100 \times 0.04 - 100 \times 0.09 - 100 \times 0.06 \\ &= 6.5 \text{ }^\circ\text{C} \end{aligned}$$

$$T_j = 75 + 6.5 = 81.5 \text{ }^\circ\text{C}$$

Hence the peak value of  $T_j$  is 143 °C for the repetitive case and 81.5 °C for the single shot case. To calculate the average junction temperature  $T_{j(av)}$ :

$$\begin{aligned} P_{av} &= \frac{3 \times 100 \times 20}{240} \\ &= 25 \text{ W} \end{aligned}$$

$$\begin{aligned} \Delta T_{j-mb(av)} &= P_{av} \times Z_{th-mb} (\delta = 1) \\ &= 25 \times 2 = 50 \text{ }^\circ\text{C} \end{aligned}$$

$$\Delta T_{j(av)} = 75 + 50 = 125 \text{ }^\circ\text{C}$$

The above example for the repetitive waveform highlights a case where the average junction temperature (125 °C) is well within limits but the composite pulse calculation shows the peak junction temperature to be significantly higher. For reasons of improved long term reliability it is usual to operate devices with a peak junction temperature below 125 °C.

## Non-rectangular pulses

So far, the worked examples have only covered rectangular waveforms. However, triangular, trapezoidal and sinusoidal waveforms are also common. In order to apply the above thermal calculations to non rectangular waveforms, the waveform is approximated by a series of rectangles. Each rectangle represents part of the waveform. The equivalent rectangle must be equal in area to the section of the waveform it represents (i.e. the same energy) and also be of the same peak power. With reference to Fig.16, a triangular waveform has been approximated to one rectangle in the first example, and two rectangles in the second. Obviously, increasing the number of sections the waveform is split into will improve the accuracy of the thermal calculations.

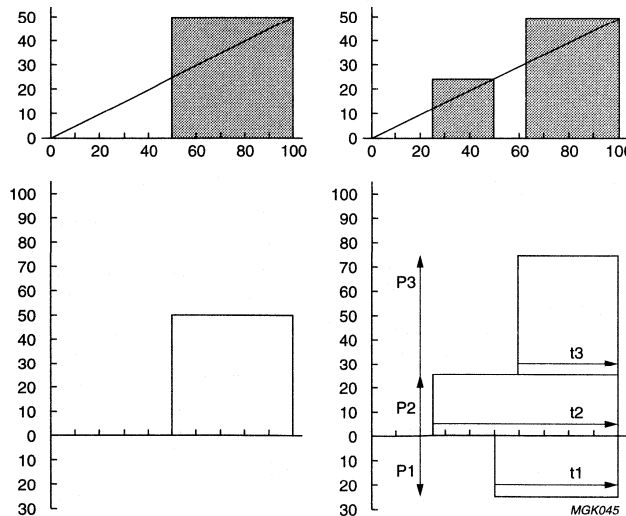


Fig.16 Non-rectangular waveform.

## Thermal considerations

## Chapter 5

In the first example, there is only one rectangular pulse, of duration 50  $\mu\text{s}$ , dissipating 50 W. So again using Equation (14) and a rearrangement of Equation (7):

$$\Delta T_{j-mb} = P_{\text{tot M}} \times Z_{\text{thj-mb}}$$

Single shot:

$$\Delta T_{j-mb} = 50 \times 0.065 = 3.25 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 3.25 = 78.5 \text{ }^\circ\text{C}$$

10% duty cycle:

$$\Delta T_{j-mb} = 50 \times 0.230 = 11.5 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 11.5 = 86.5 \text{ }^\circ\text{C}$$

50% duty cycle:

$$\Delta T_{j-mb} = 50 \times 1.000 = 50 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 50 = 125 \text{ }^\circ\text{C}$$

When the waveform is split into two rectangular pulses:

$$\Delta T_{j-mb} = P_3 \times Z_{\text{thj-mb}}(t_3) + P_1 \times Z_{\text{thj-mb}}(t_2) - P_2 \times Z_{\text{thj-mb}}(t_2) \quad (16)$$

For this example  $P_1 = 25 \text{ W}$ ,  $P_2 = 25 \text{ W}$ ,  $P_3 = 50 \text{ W}$ . Table 4 shows the rest of the parameters.

**Table 4** Non-rectangular pulse calculations

		t1	t2	t3
		75 $\mu\text{s}$	50 $\mu\text{s}$	37.5 $\mu\text{s}$
Single shot	$\delta$	0.000	0.000	0.000
$T = \infty$	$Z_{\text{th}}$	0.085	0.065	0.055
10% duty cycle	$\delta$	0.075	0.050	0.037
$T = 1000 \mu\text{s}$	$Z_{\text{th}}$	0.210	0.140	0.120
50% duty cycle	$\delta$	0.375	0.250	0.188
$T = 200 \mu\text{s}$	$Z_{\text{th}}$	0.700	0.500	0.420

Substituting these values into Equation (18) gives:

Single shot:

$$\Delta T_{j-mb} = 50 \times 0.055 + 25 \times 0.85 - 25 \times 0.65 = 3.25 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 3.25 = 78.5 \text{ }^\circ\text{C}$$

10% Duty cycle

$$\Delta T_{j-mb} = 50 \times 0.12 + 25 \times 0.21 - 25 \times 0.14 = 7.75 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 7.75 = 82.5 \text{ }^\circ\text{C}$$

50% Duty cycle

$$\Delta T_{j-mb} = 50 \times 0.42 + 25 \times 0.7 - 25 \times 0.5 = 26 \text{ }^\circ\text{C}$$

$$\Delta T_{j\text{peak}} = 75 + 26 = 101 \text{ }^\circ\text{C}$$

To calculate the average junction temperature:

$$P_{\text{av}} = \frac{50 \times 50}{1000} = 2.5 \text{ W}$$

$$\Delta T_{j-mb(\text{av})} = P_{\text{av}} \times Z_{\text{th-mb}}(\delta = 1) = 2.5 \times 2 = 5 \text{ }^\circ\text{C}$$

$$\Delta T_{j(\text{av})} = 75 + 5 = 80 \text{ }^\circ\text{C}$$

### Conclusion to part two

A method has been presented to allow the calculation of average and peak junction temperatures for a variety of pulse types. Several worked examples have shown calculations for various common waveforms. The method for non-rectangular pulses can be applied to any wave shape, allowing temperature calculations for waveforms such as exponential and sinusoidal power pulses. For pulses such as these, care must be taken to ensure that the calculation gives the peak junction temperature, as it may not occur at the end of the pulse. In this instance several calculations must be performed with different endpoints to find the maximum junction temperature.

## Thermal considerations

## Chapter 5

## PART 3: HEAT DISSIPATION

All semiconductor failure mechanisms are temperature dependent and so the lower the junction temperature, the higher the reliability of the circuit. Thus our data specifies a maximum junction temperature which should not be exceeded under the worst probable conditions. However, derating the operating temperature from  $T_{jmax}$  is always desirable to improve the reliability still further. The junction temperature depends on both the power dissipated in the device and the thermal resistances (or impedances) associated with the device. Thus careful consideration of these thermal resistances (or impedances) allows the user to calculate the maximum power dissipation that will keep the junction temperature below a chosen value.

The formulae and diagrams given in this part can only be considered as a guide for determining the nature of a heatsink. This is because the thermal resistance of a heatsink depends on numerous parameters which cannot be predetermined. They include the position of the transistor on the heatsink, the extent to which air can flow unhindered, the ratio of the lengths of the sides of the heatsink, the screening effect of nearby components, and heating from these components. It is always advisable to check important temperatures in the finished equipment under the worst probable operating conditions. The more complex the heat dissipation conditions, the more important it becomes to carry out such checks.

## Heat flow path

The heat generated in a semiconductor chip flows by various paths to the surroundings. Small signal devices do not usually require heatsinking; the heat flows from the junction to the mounting base which is in close contact with the case. Heat is then lost by the case to the surroundings by convection and radiation (Fig. 17a). Power transistors, however, are usually mounted on heatsinks because of the higher power dissipation they experience. Heat flows from the transistor case to the heatsink by way of contact pressure, and the heatsink loses heat to the surroundings by convection and radiation, or by conduction to cooling water (Fig. 17b). Generally air cooling is used so that the ambient referred to in Fig. 17 is usually the surrounding air. Note that if this is the air inside an equipment case, the additional thermal resistance between the inside and outside of the equipment case should be taken into account.

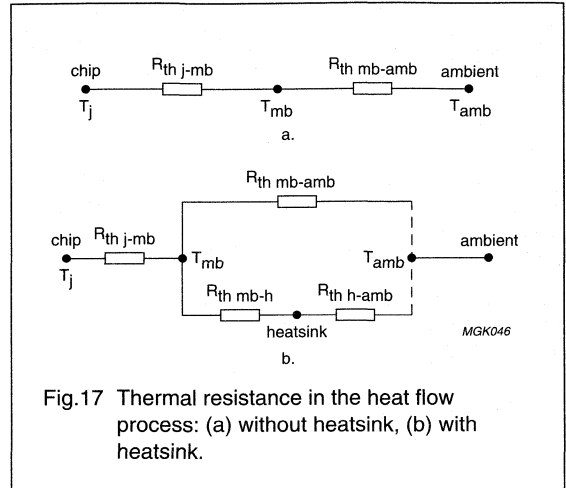


Fig. 17 Thermal resistance in the heat flow process: (a) without heatsink, (b) with heatsink.

Contact thermal resistance  $R_{th\ mb-h}$ 

The thermal resistance between the transistor mounting base and the heatsink depends on the quality and size of the contact areas, the type of any intermediate plates used, and the contact pressure. Care should be taken when drilling holes in heatsinks to avoid burring and distorting the metal, and both mating surfaces should be clean. Paint finishes of normal thickness, up to 50  $\mu\text{m}$  (as a protection against electrolytic voltage corrosion), barely affect the thermal resistance. Transistor case and heatsink surfaces can never be perfectly flat, and so contact will take place on several points only, with a small air-gap over the rest of the area. The use of a soft substance to fill this gap lowers the contact thermal resistance. Normally, the gap is filled with a heatsinking compound which remains fairly viscous at normal transistor operating temperatures and has a high thermal conductivity. The use of such a compound also prevents moisture from penetrating between the contact surfaces. Proprietary heatsinking compounds are available which consist of a silicone grease loaded with some electrically insulating good thermally conducting powder such as alumina. The contact thermal resistance  $R_{th\ mb-h}$  is usually small with respect to  $(R_{th\ j-mb} + R_{th\ h-amb})$  when cooling is by natural convection. However, the heatsink thermal resistance  $R_{th\ h-amb}$  can be very small when either forced ventilation or water cooling are used, and thus a close thermal contact between the transistor case and heatsink becomes particularly important.



## Thermal considerations

## Chapter 5

## Thermal resistance calculations

Fig.17a shows that, when a heatsink is not used, the total thermal resistance between junction and ambient is given by:

$$R_{th\ j-amb} = R_{th\ j-mb} + R_{th\ mb-amb} \quad (17)$$

However, power transistors are generally mounted on a heatsink since  $R_{th\ j-amb}$  is not usually small enough to maintain temperatures within the chip below desired levels.

Fig.17b shows that, when a heatsink is used, the total thermal resistance is given by:

$$R_{th\ j-amb} = R_{th\ j-mb} + R_{th\ mb-h} + R_{th\ h-amb} \quad (18)$$

Note that the direct heat loss from the transistor case to the surroundings through  $R_{th\ mb-amb}$  is negligibly small.

The first stage in determining the size and nature of the required heatsink is to calculate the maximum heatsink thermal resistance  $R_{th\ h-amb}$  that will maintain the junction temperature below the desired value.

## Continuous operation

Under DC conditions, the maximum heatsink thermal resistance can be calculated directly from the maximum desired junction temperature.

$$R_{th\ j-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} \quad (19)$$

and

$$R_{th\ j-mb} = \frac{T_j - T_{mb}}{P_{tot(av)}} \quad (20)$$

Combining Equations (18) and (19) gives:

$$R_{th\ h-amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} - R_{th\ j-mb} - R_{th\ mb-h} \quad (21)$$

and substituting Equation (20) into Equation (21) gives:

$$R_{th\ h-amb} = \frac{T_{mb} - T_{amb}}{P_{tot(av)}} - R_{th\ mb-h} \quad (22)$$

The values of  $R_{th\ j-mb}$  and  $R_{th\ mb-h}$  are given in the published data. Thus, either Equation (21) or Equation (22) can be used to find the maximum heatsink thermal resistance.

## Intermittent operation

The thermal equivalent circuits of Fig.17 are inappropriate for intermittent operation, and the thermal impedance  $Z_{th\ j-mb}$  should be considered.

$$P_{totM} = \frac{T_j - T_{mb}}{Z_{th\ j-mb}}$$

thus:

$$T_{mb} = T_j - P_{totM} \times Z_{th\ j-mb} \quad (23)$$

The mounting-base temperature has always been assumed to remain constant under intermittent operation. This assumption is known to be valid in practice provided that the pulse time is less than about one second. The mounting-base temperature does not change significantly under these conditions as indicated in Fig.18. This is because heatsinks have a high thermal capacity and thus a high thermal time-constant.

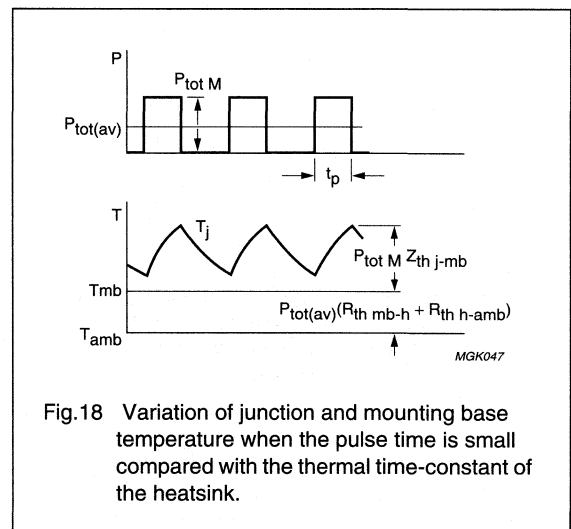


Fig.18 Variation of junction and mounting base temperature when the pulse time is small compared with the thermal time-constant of the heatsink.

Thus Equation (22) is valid for intermittent operation, provided that the pulse time is less than one second. The value of  $T_{mb}$  can be calculated from Equation (23), and the heatsink thermal resistance can be obtained from Equation (22).

## Thermal considerations

## Chapter 5

The thermal time constant of a transistor is defined as that time at which the junction temperature has reached 70% of its final value after being subjected to a constant power dissipation at a constant mounting base temperature.

Now, if the pulse duration  $t_p$  exceeds one second, the transistor is temporarily in thermal equilibrium since such a pulse duration is significantly greater than the thermal time-constant of most transistors. Consequently, for pulse times of more than one second, the temperature difference  $T_j - T_{mb}$  reaches a stationary final value (Fig.19) and Equation (23) should be replaced by:

$$T_{mb} = T_j - P_{totM} \times R_{th j-mb} \quad (24)$$

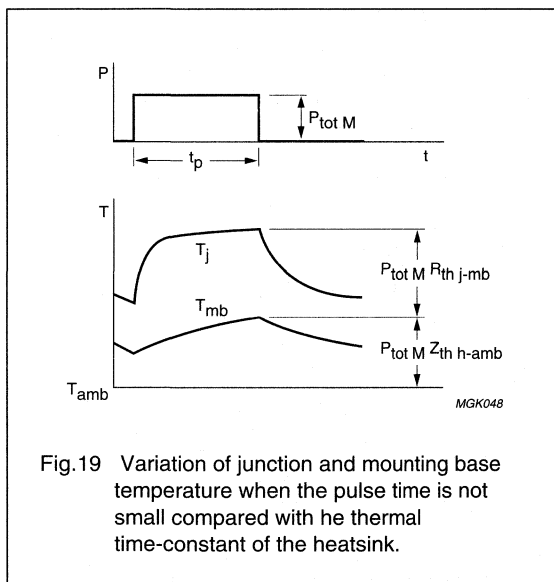


Fig.19 Variation of junction and mounting base temperature when the pulse time is not small compared with the thermal time-constant of the heatsink.

In addition, it is no longer valid to assume that the mounting base temperature is constant since the pulse time is also no longer small with respect to the thermal time constant of the heatsink.

### Smaller heatsinks for intermittent operation

In many instances, the thermal capacity of a heatsink can be utilized to design a smaller heatsink for intermittent operation than would be necessary for the same level of continuous power dissipation. The average power dissipation in Equation (22) is replaced by the peak power dissipation to obtain the value of the thermal impedance between the heatsink and the surroundings.

$$Z_{th h-amb} = \frac{T_{mb} - T_{amb}}{P_{totM}} - R_{th mb-h} \quad (25)$$

The value of  $Z_{th h-amb}$  will be less than the comparable thermal resistance and thus a smaller heatsink can be designed than that obtained using the too large value calculated from Equation (22).

### Heatsinks

Three varieties of heatsink are in common use: flat plates (including chassis), diecast finned heatsinks, and extruded finned heatsinks. The material normally used for heatsink construction is aluminium although copper may be used with advantage for flat-sheet heatsinks. Small finned clips are sometimes used to improve the dissipation of low-power transistors.

### Heatsink finish

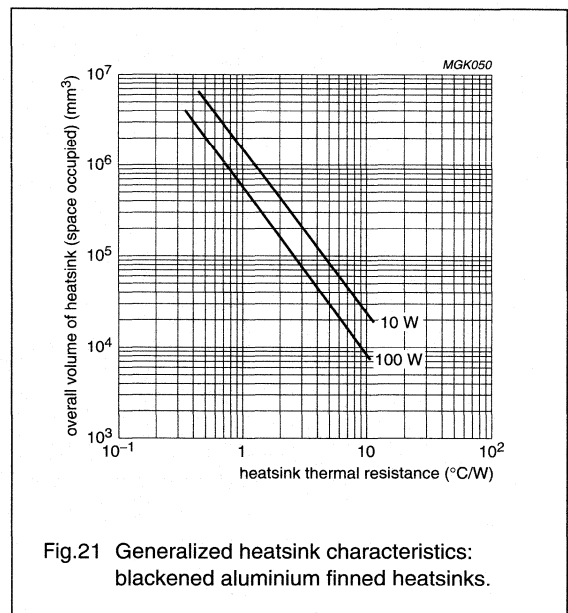
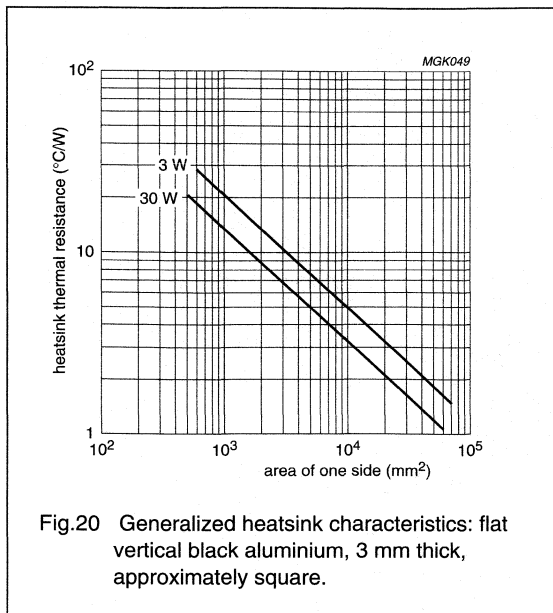
Heatsink thermal resistance is a function of surface finish. A painted surface will have a greater emissivity than a bright unpainted one. The effect is most marked with flat plate heatsinks, where about one third of the heat is dissipated by radiation. The colour of the paint used is relatively unimportant, and the thermal resistance of a flat plate heatsink painted gloss white will be only about 3% higher than that of the same heatsink painted matt black. With finned heatsinks, painting is less effective since heat radiated from most fins will fall on adjacent fins but it is still worthwhile. Both anodising and etching will decrease the thermal resistivity. Metallic type paints, such as aluminium paint, have the lowest emissivities, although they are approximately ten times better than a bright aluminium metal finish.

### Flat-plate heatsinks

The simplest type of heatsink is a flat metal plate to which the transistor is attached. Such heatsinks are used both in the form of separate plates and as the equipment chassis itself. The thermal resistance obtained depends on the thickness, area and orientation of the plate, as well as on the finish and power dissipated. A plate mounted horizontally will have about twice the thermal resistance of a vertically mounted plate. This is particularly important where the equipment chassis itself is used as the heatsink. In Fig.20, the thermal resistance of a blackened heatsink is plotted against surface area (one side) with power dissipation as a parameter. The graph is accurate to within 25% for nearly square plates, where the ratio of the lengths of the sides is less than 1.25:1.

Thermal considerations

Chapter 5



**Finned heatsinks**

Finned heatsinks may be made by stacking flat plates, although it is usually more economical to use ready made diecast or extruded heatsinks. Since most commercially available finned heatsinks are of reasonably optimum design, it is possible to compare them on the basis of the overall volume which they occupy. This comparison is made in Fig.21 for heatsinks with their fins mounted vertically; again, the graph is accurate to 25%.

**Heatsink dimensions**

The maximum thermal resistance through which sufficient power can be dissipated without damaging the transistor can be calculated as discussed previously. This section explains how to arrive at a type and size of heatsink that gives a sufficiently low thermal resistance.

**Natural air cooling**

The required size of aluminium heatsinks - whether flat or extruded (finned) can be derived from the nomogram in Fig.22. Like all heatsink diagrams, the nomogram does not give exact values for  $R_{th\ h-amb}$  as a function of the dimensions since the practical conditions always deviate to some extent from those under which the nomogram was drawn up. The actual values for the heatsink thermal resistance may differ by up to 10% from the nomogram values. Consequently, it is advisable to take temperature measurements in the finished equipment, particularly where the thermal conditions are critical.

Thermal considerations

Chapter 5

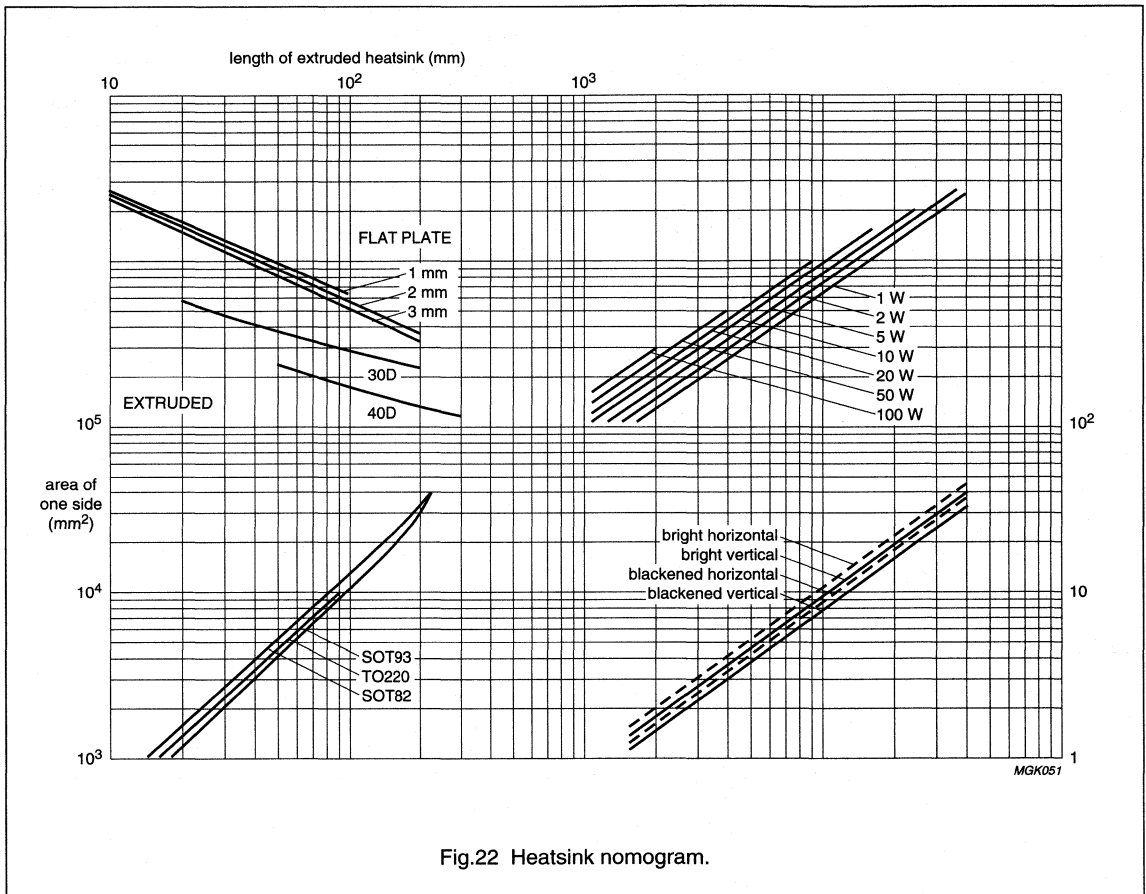


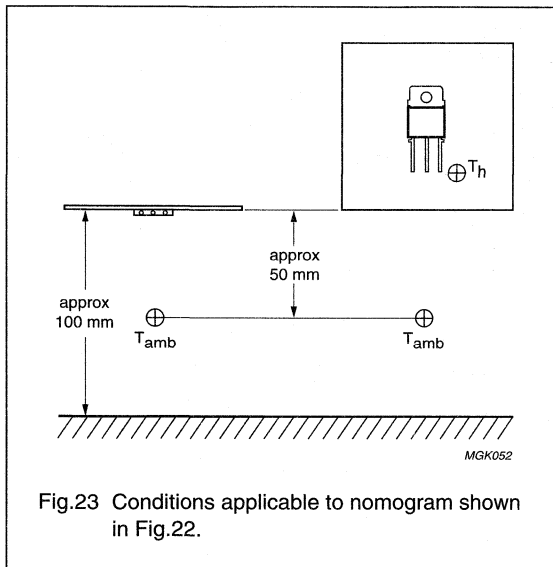
Fig.22 Heatsink nomogram.

# Thermal considerations

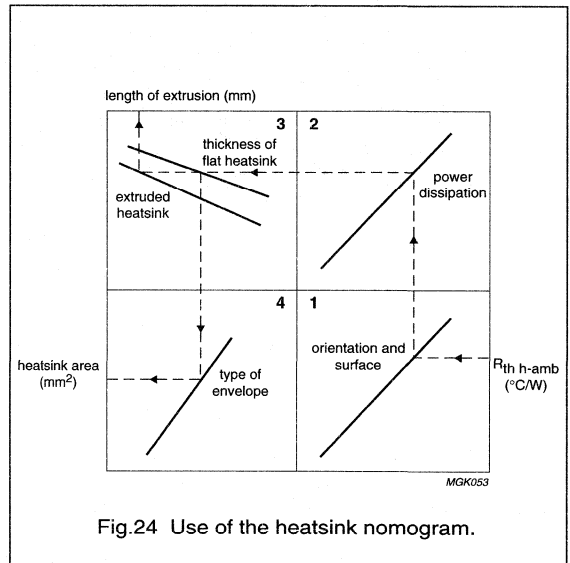
# Chapter 5

The conditions to which the nomogram applies are as follows:

- natural air cooling (unimpeded natural convection with no build up of heat)
- ambient temperature about 25 °C, measured about 50 mm below the lower edge of the heatsink (see Fig.23)
- single mounting (that is, not affected by nearby heatsinks)
- atmospheric pressure about 10 N/m<sup>2</sup>
- distance between the bottom of the heatsink and the base of a draught-free space about 100 mm (see Fig.23)
- transistor mounted roughly in the centre of the heatsink (this is not so important for finned heatsinks because of the good thermal conduction).



4. If an extruded heatsink is required, move vertically upwards to obtain its length (Figs 25a and 25b give the outlines of the extrusions).
5. If a flat-plate heatsink is to be used, move vertically downwards to intersect the appropriate curve for envelope type in section 4.
6. Move horizontally to the left to obtain heatsink area.
7. The heatsink dimensions should not exceed the ratio of 1.25:1.

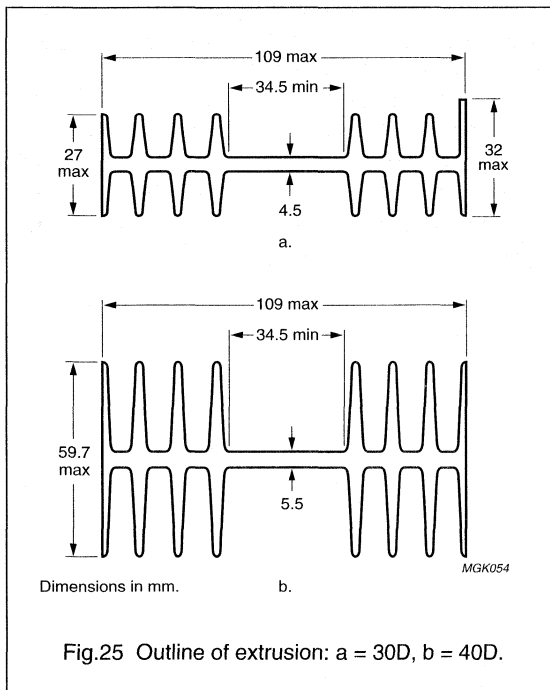


The appropriately-sized heatsink is found as follows.

1. Enter the nomogram from the right hand side of section 1 at the appropriate  $R_{th h-amb}$  value (see Fig.24). Move horizontally to the left, until the appropriate curve for orientation and surface finish is reached.
2. Move vertically upwards to intersect the appropriate power dissipation curve in section 2.
3. Move horizontally to the left into section 3 for the desired thickness of a flat-plate heatsink, or the type of extrusion.

## Thermal considerations

## Chapter 5



The curves in section 2 take account of the non linear nature of the relationship between the temperature drop across the heatsink and the power dissipation loss. Thus, at a constant value of the heatsink thermal resistance, the greater the power dissipation, the smaller is the required size of heatsink. This is illustrated by the following example.

**Example**

An extruded heatsink mounted vertically and with a painted surface is required to have a maximum thermal resistance of  $R_{th\ h-amb} = 2.6\ ^\circ\text{C}/\text{W}$  at the following powers:

a)  $P_{tot(av)} = 5\ \text{W}$

b)  $P_{tot(av)} = 50\ \text{W}$

Enter the nomogram at the appropriate value of the thermal resistance in section 1, and via either the 50 W or 5 W line in section 2, the appropriate lengths of the extruded heatsink 30D are found to be:

a) length = 110 mm

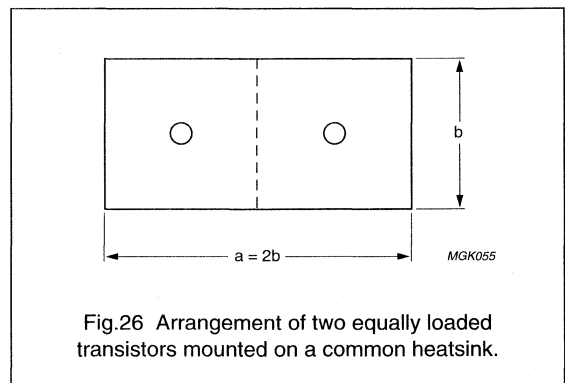
b) length = 44 mm

Case (b) requires a shorter length since the temperature difference is ten times greater than in case (a).

As the ambient temperature increases beyond  $25\ ^\circ\text{C}$ , so does the temperature of the heatsink and thus the thermal resistance (at constant power) decreases owing to the increasing role of radiation in the heat removal process. Consequently, a heatsink with dimensions derived from Fig.22 at  $T_{amb} > 25\ ^\circ\text{C}$  will be more than adequate. If the maximum ambient temperature is less than  $25\ ^\circ\text{C}$ , then the thermal resistance will increase slightly. However, any increase will lie within the limits of accuracy of the nomogram and within the limits set by other uncertainties associated with heatsink calculations.

For heatsinks with relatively small areas, a considerable part of the heat is dissipated from the transistor case. This is why the curves in section 4 tend to flatten out with decreasing heatsink area. The area of extruded heatsinks is always large with respect to the surface of the transistor case, even when the length is small.

If several transistors are mounted on a common heatsink, each transistor should be associated with a particular section of the heatsink (either an area or length according to type) whose maximum thermal resistance is calculated from Equations (21) or (22); that is, without taking the heat produced by nearby transistors into account. From the sum of these areas or lengths, the size of the common heatsink can then be obtained. If a flat heatsink is used, the transistors are best arranged as shown in Fig.26. The maximum mounting base temperatures of transistors in such a grouping should always be checked once the equipment has been constructed.



## Thermal considerations

## Chapter 5

**Forced air cooling**

If the thermal resistance needs to be much less than  $1\text{ }^{\circ}\text{C}/\text{W}$ , or the heatsink not too large, forced air cooling by means of fans can be provided. Apart from the size of the heatsink, the thermal resistance now only depends on the speed of the cooling air. Provided that the cooling air flows parallel to the fins and with sufficient speed ( $>0.5\text{ m/s}$ ), the thermal resistance hardly depends on the power dissipation and the orientation of the heatsink. Note that turbulence in the air current can result in practical values deviating from theoretical values.

Figure 27 shows the form in which the thermal resistances for forced air cooling are given in the case of extruded heatsinks. It also shows the reduction in thermal resistance or length of heatsink which may be obtained with forced air cooling.

The effect of forced air cooling in the case of flat heatsinks is seen from Fig.28. Here, too, the dissipated power and the orientation of the heatsink have only a slight effect on the thermal resistance, provided that the air flow is sufficiently fast.

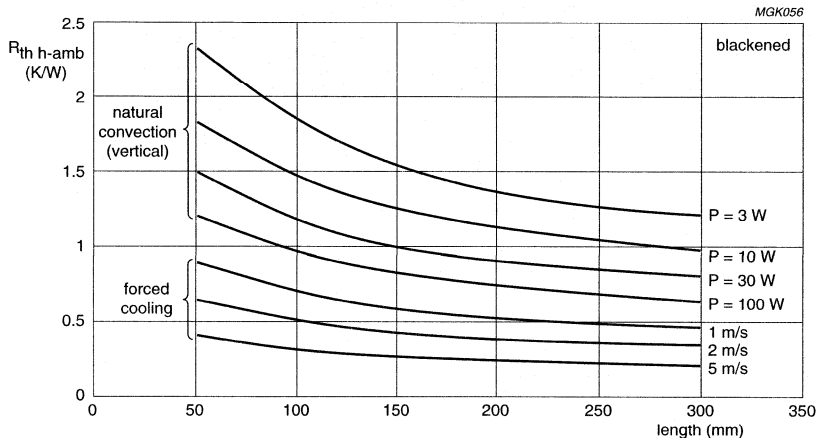


Fig.27 Thermal resistance of a finned heatsink (type 40D) as a function of the length, with natural and forced air cooling.

Thermal considerations

Chapter 5

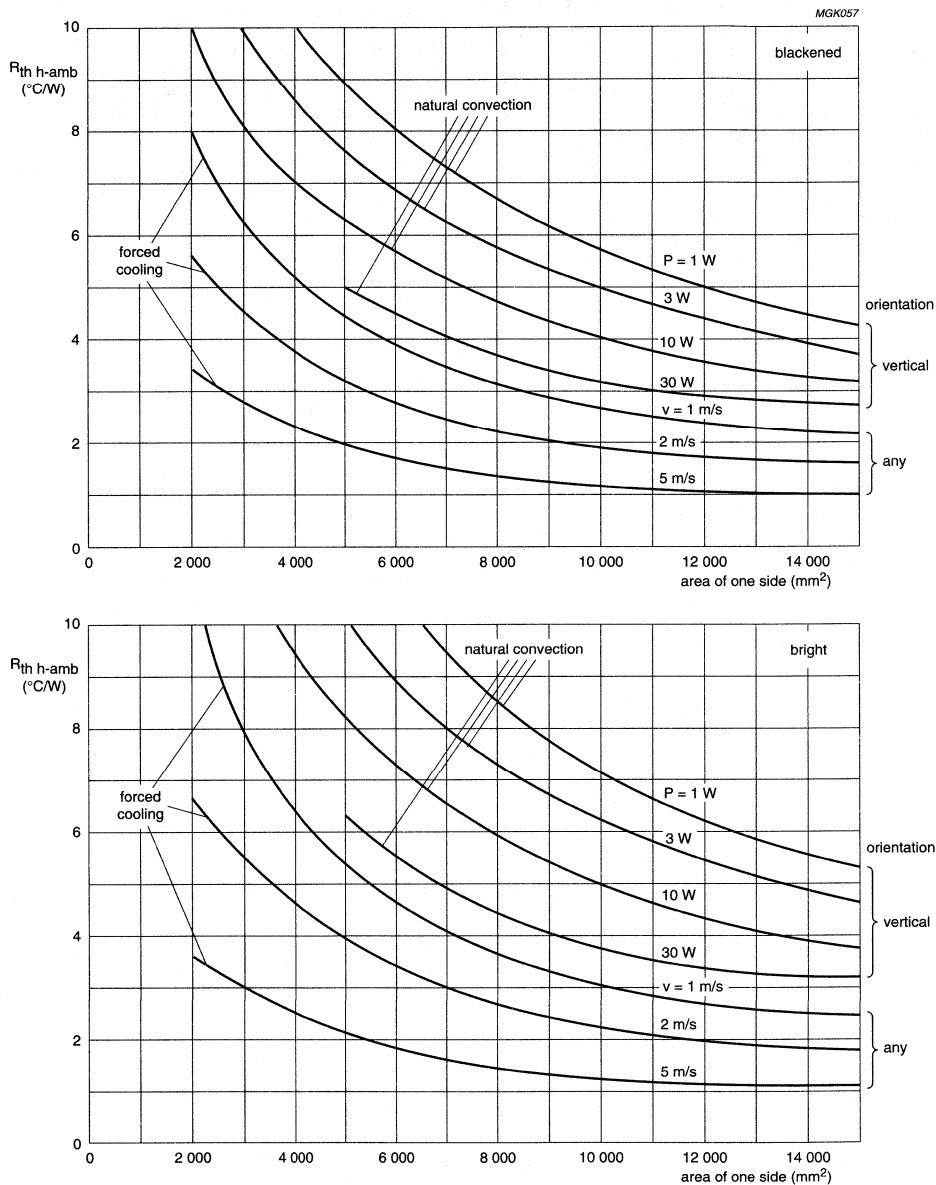


Fig.28 Thermal resistance of heatsinks (2 mm thick copper or 3 mm aluminium) under natural convection and forced cooling conditions, with a SOT93 package.



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## Thermal considerations

## Chapter 5

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### **Conclusion to part three**

The majority of power transistors require heatsinking, and when the maximum thermal resistance that will maintain the device's junction temperature below its rating has been calculated, a heatsink of appropriate type and size can be chosen. The practical conditions under which a transistor

will be operated are likely to differ from the theoretical considerations used to determine the required heatsink, and so temperatures should always be checked in the finished equipment. Finally, some applications require a small heatsink, or one with a very low thermal resistance, in which case forced air cooling by means of fans should be provided.



## Packing Methods

## Chapter 6

### INTRODUCTION

This chapter contains a survey of some of the packing methods most frequently used by Philips Semiconductors. It includes information that may be important to customers when making their purchasing decisions, for example the main dimensions, shapes, and packing quantities.

### Standardization

For semiconductors, packing serves two important functions. The first and most obvious function is protection during storage and transport to customers. This, of course, applies to all products, not just semiconductors. The second is to act as a delivery medium for automatic placement machines during equipment manufacture. To do this effectively, the reels, trays and tubes that components are packed in must meet recognized standards. In this respect, Philips Semiconductors actively cooperates with standardization authorities throughout the world.

In addition, our packing methods meet all major international standards, including those of IEC (International Electrotechnical Commission), JEDEC (Joint Electron Device Engineering Council, USA) and NEDA (National Electronic Distributor Association, USA).

### Environmental care

Nowadays, an important issue is environmental impact. Component and equipment manufacturers are continuously working to improve the environment friendliness of their products and packing, and have devoted much effort to eliminating the use of toxic materials and to looking at ways in which materials can be recycled.

In these respects, Philips Semiconductors has taken several important steps on the packing front. These include:

- Reducing the amount of packing material by switching to 'one piece' boxes (instead of boxes with upper and lower parts)
- Changing to 'mono material' to aid recycling. For example, from aluminium-lined boxes to carbon-coated boxes.
- Changing from white boxes to natural brown boxes to eliminate the use of bleach (chlorine) in their manufacture.

The aim is minimum waste and minimum environmental impact. We have already gone a long way towards this in the development of our packing methods. And future developments will take us even further along this route.

### More Information

For more information about packing methods, please contact:

Philips Semiconductors Packing Management,  
BAE-09  
P.O. Box 218,  
5600 MD Eindhoven  
The Netherlands.

### GLOSSARY OF TERMS

Carrier	Plastic tube, tray or tape with cavities, which can contain IC products
Package	Container with leads for an IC chip (also known as an envelope or outline)
Packing method	Combination of a carrier and a box to protect products during transport and storage
Pin	Rigid plastic pin that closes a tube for DIP packages by insertion through holes in its end
Plug	Flexible plastic plug that closes a tube for PLCC or SIL packages by insertion into its end
PQ	Packing Quantity, in a box containing one or more SPQs
SOD	Standard Outline Diode
SOT	Standard Outline Transistor
SPQ	Smallest Packing Quantity, mostly the quantity in one carrier
Surface mount	Mounted on the surface of a PCB
Through-hole	Mounted onto a PCB by insertion of leads into holes
Turnlock	Rigid plastic pin that closes a tube for SO packages by insertion into its end and turning to lock in place

# Packing Methods

# Chapter 6

## PACKING METHODS IN EXPLODED VIEW

Item	Material	Weight <sup>(1)</sup> (g)
Box	Cardboard	346.00
Tape	Paper	75.30
Tape	Paper	108.00
Tape	Polypropylene	2.50
Labels	Paper	2.12
Clamping bush	Polystyrene	32.00
Distance hub	Paper	26.00
Flange	Paper	420.00
QA Seal	Acrylate	0.15

<sup>(1)</sup> For SOD57 (355-52)

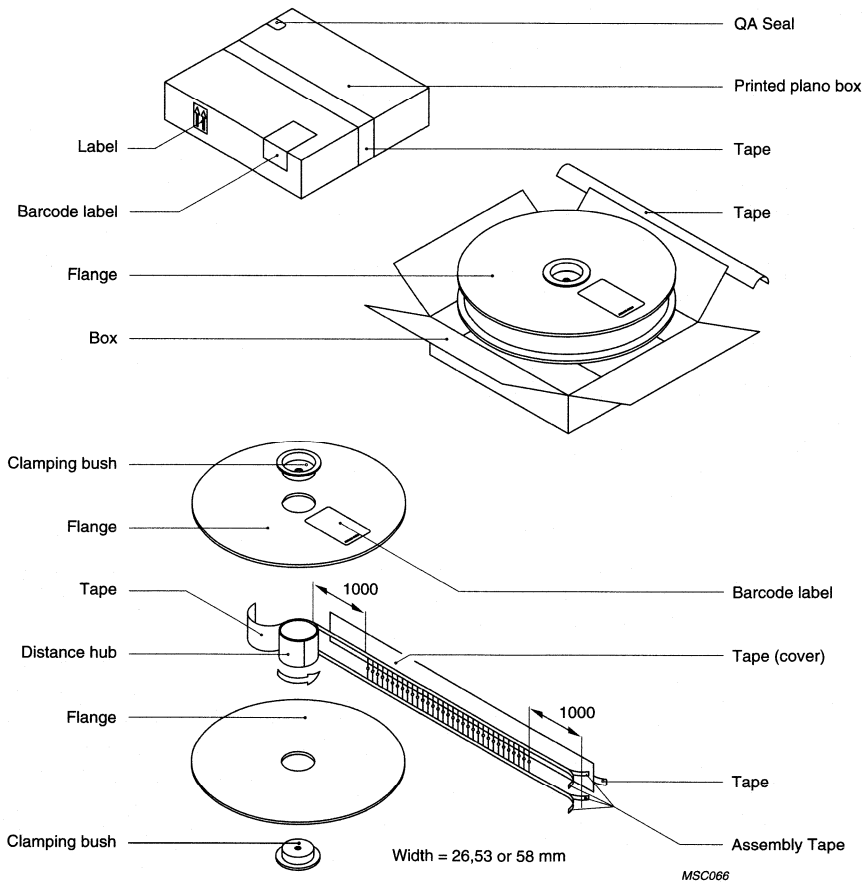


Fig.1 Reel pack axial taped.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Box	Cardboard	309.00
Assy tape	Paper	494.00
Cover tape	Paper	99.00
Tape	Polypropylene	2.00
Clamping bush	Polystyrene	32.00
Hub	Paper	32.30
Flange	Paper	170.00
Labels	Paper	1.62
QA Seal	Acrylate	0.15

<sup>(1)</sup> For SOD27 (355x42)

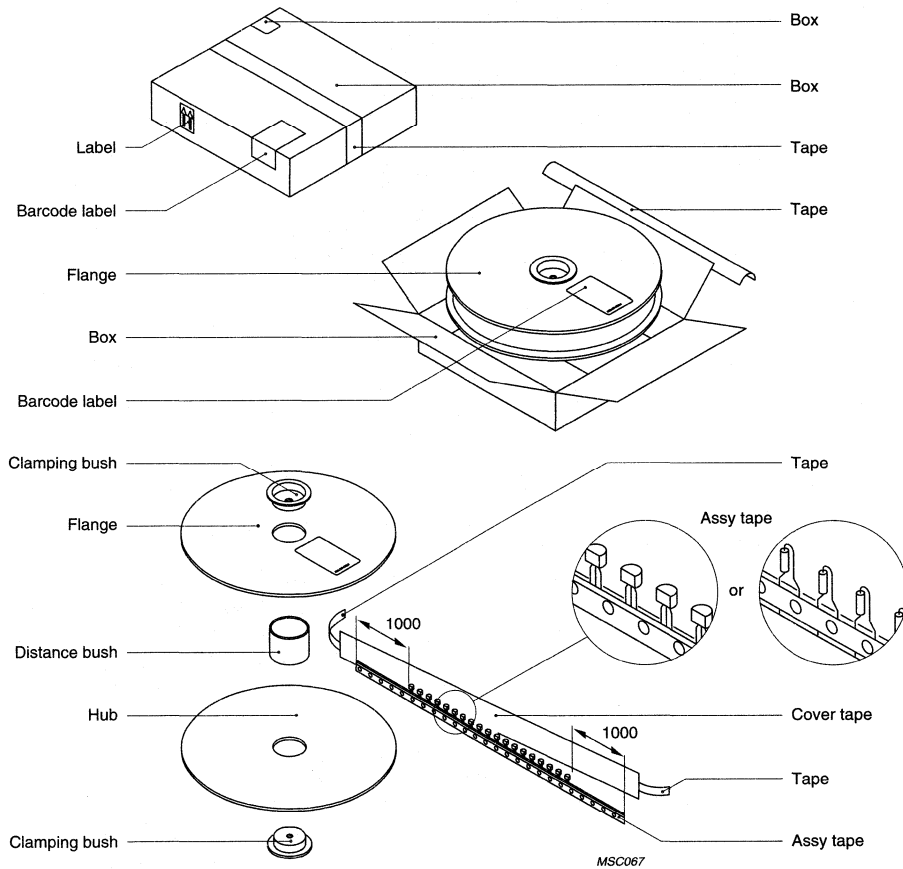


Fig.2 Reel pack radial taped.

# Packing Methods

# Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	48.00
Tape	Paper	0.18
Labels	Paper	0.91
Reel	Polystyrene	42.50
Cover tape	Polyester	3.00
Carrier tape	Polystyrene	15.40
Seal	Acrylate	0.15

<sup>(1)</sup> For SOD87 (180 x 8)

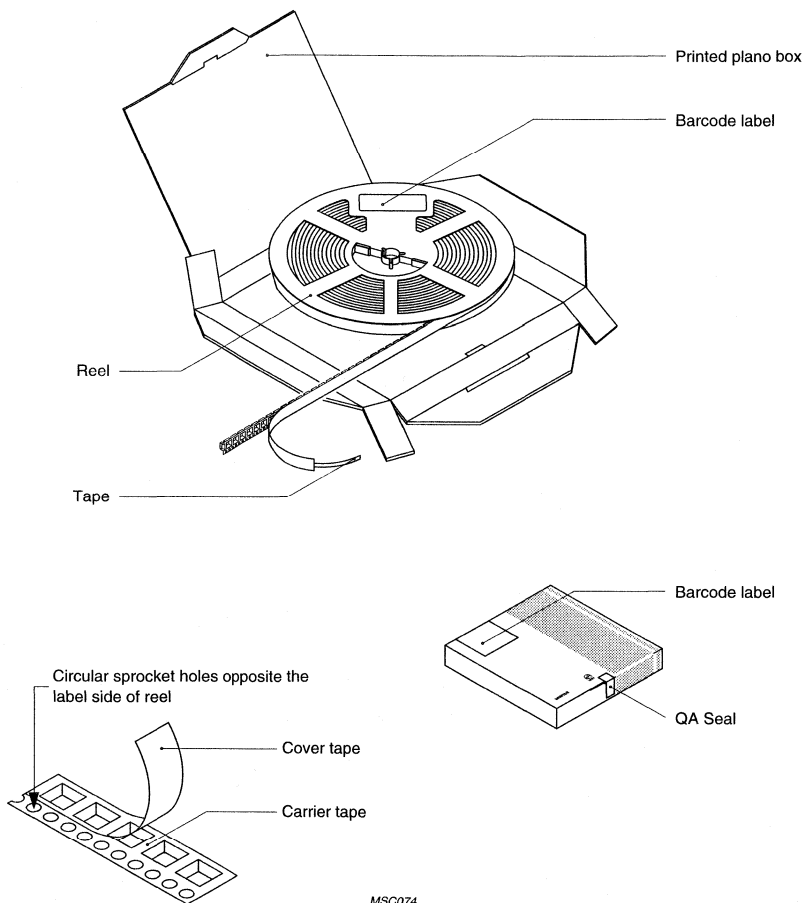


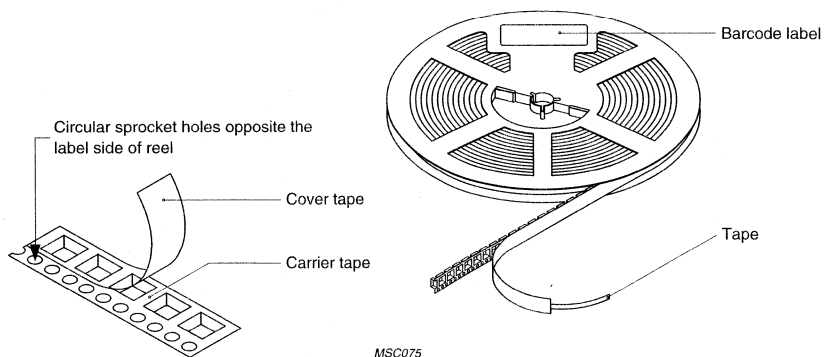
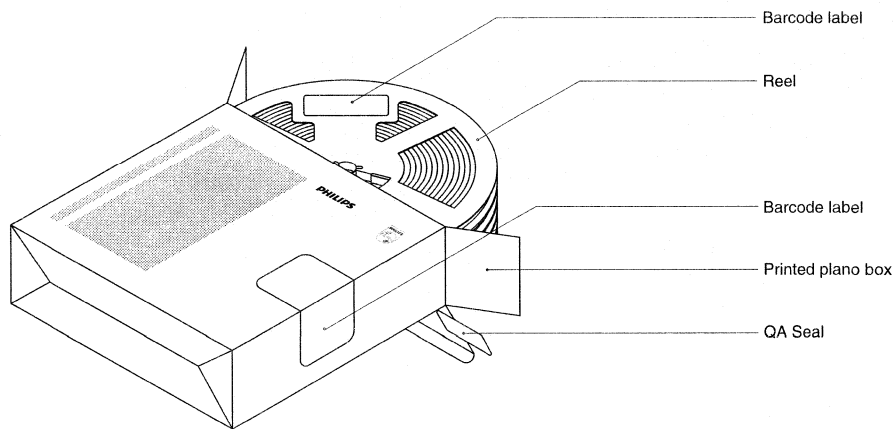
Fig.3 Reel pack for SMD.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	47.00
Tape	Paper	1.00
Labels	Paper	4.55
Reel	Polystyrene	212.50
Cover tape	Polyester	15.00
Carrier tape	Polystyrene	46.20
Seal	Acrylate	0.15

<sup>(1)</sup> For SOD87 (180 x 8)



MSC075

Fig.4 Five reel pack for SMD.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	522.50
Tape	Polypropylene	24.30
Label	Paper	4.26
Bag	Polyethylene	60.00
Seal	Acrylate	0.15
Plate	Cardboard	78.00
Box	Cardboard	435.00

<sup>(1)</sup> For SOT54

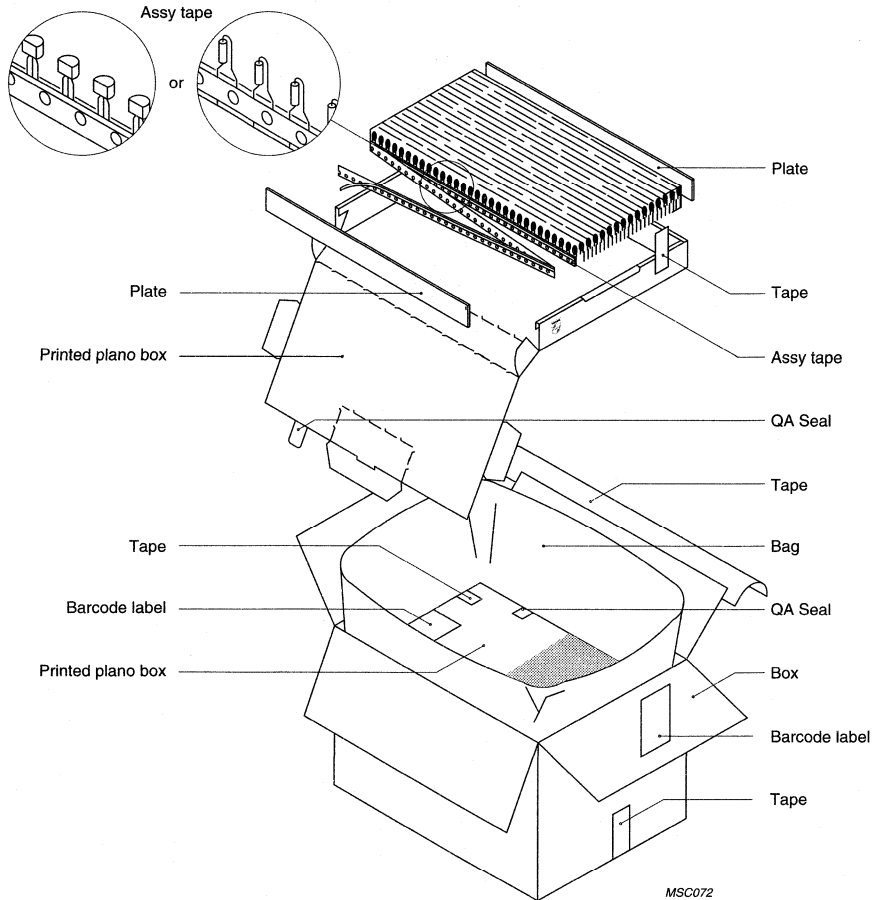


Fig.5 Five ammo pack radial taped.

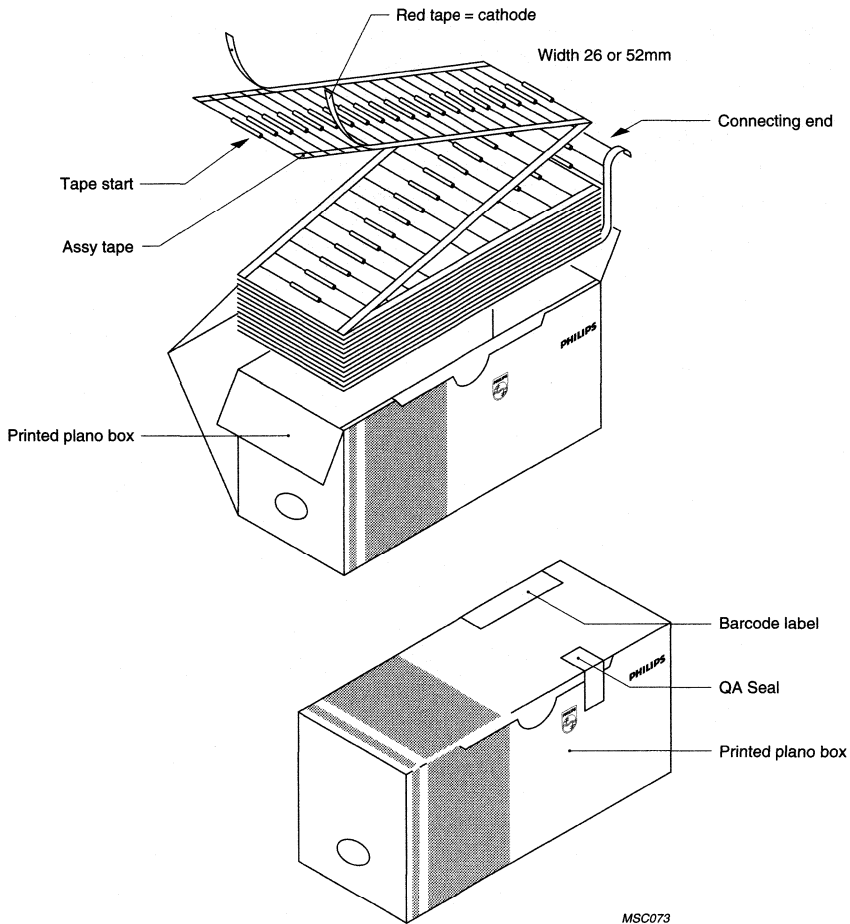


Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	40.00
Assy tape	Paper	32.49
Labels	Paper	0.71
Tape	Polypropylene	0.25
QA Seal	Acrylate	0.15

<sup>(1)</sup> For SOD84 52mm



MSC073

Fig.6 Ammo pack axial taped.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	20.25
Assy tape	Paper	2.60
Labels	Paper	0.71
Seal	Acrylate	0.15

<sup>(1)</sup> For SOD84 52mm

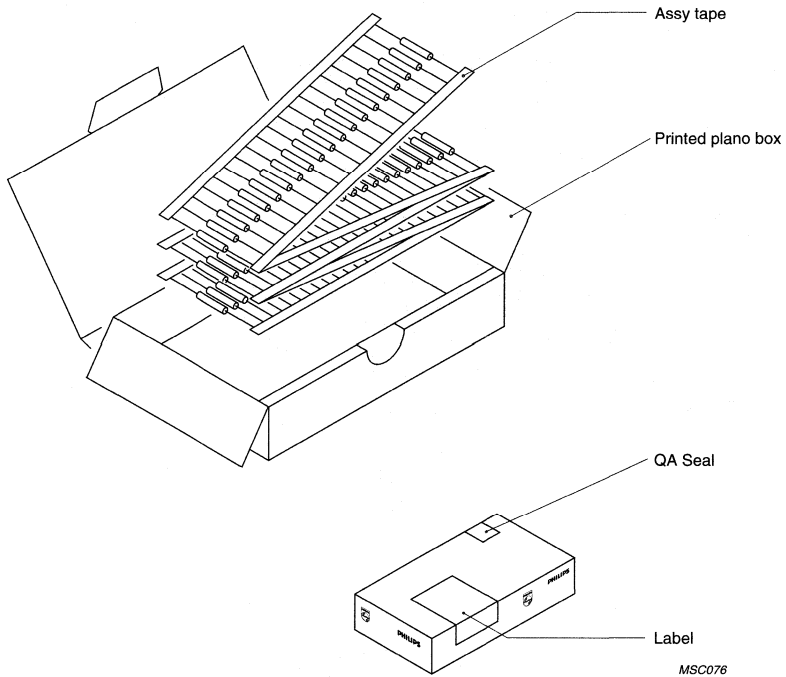


Fig.7 Ammo pack axial taped small size.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	112.00
Tape	Polypropylene	0.10
Labels	Paper	2.53
Foam	Polyethylene	6.10
Blister	Polystyrene	92.00
Seal	Acrylate	0.45

<sup>(1)</sup> For SOT147

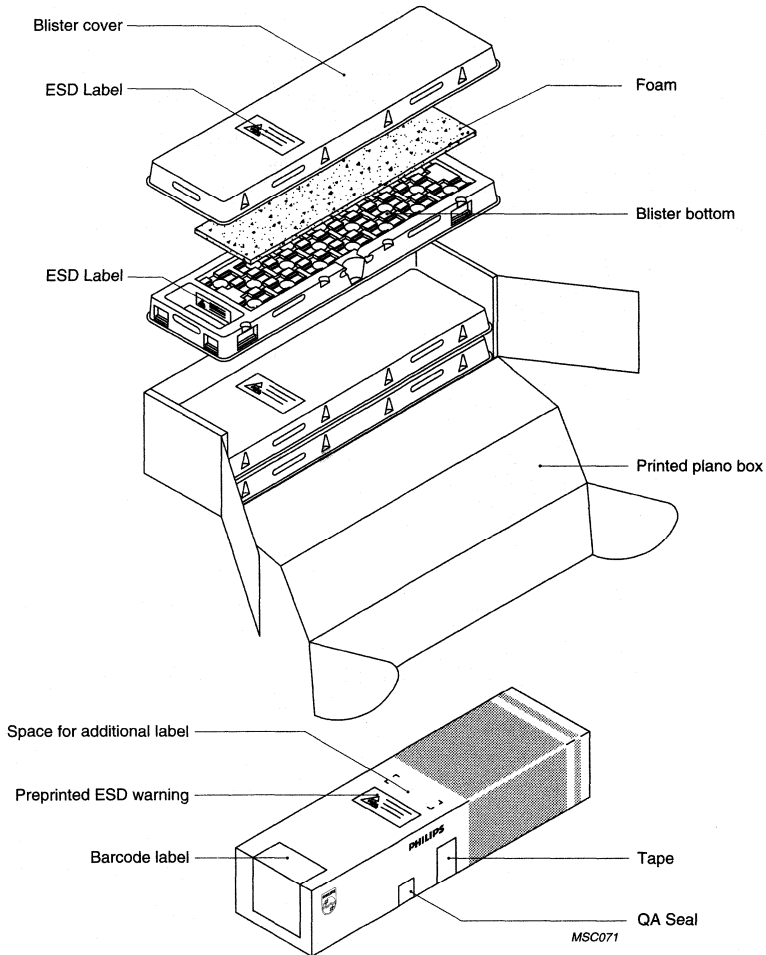


Fig.8 Blister pack.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	155.00
Tape	Polypropylene	0.10
Labels	Paper	28.71
Tube	Polyvinylchloride	720.00
Turnlock	Polyamide	24.00
Seal	Acrylate	0.15

<sup>(1)</sup> For SOT78

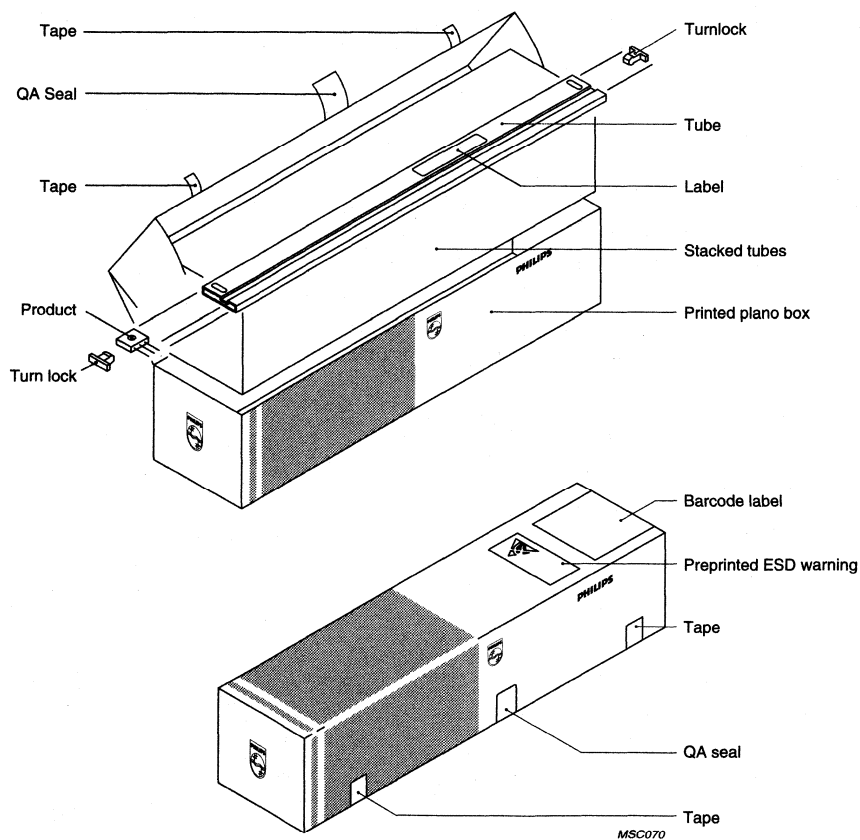


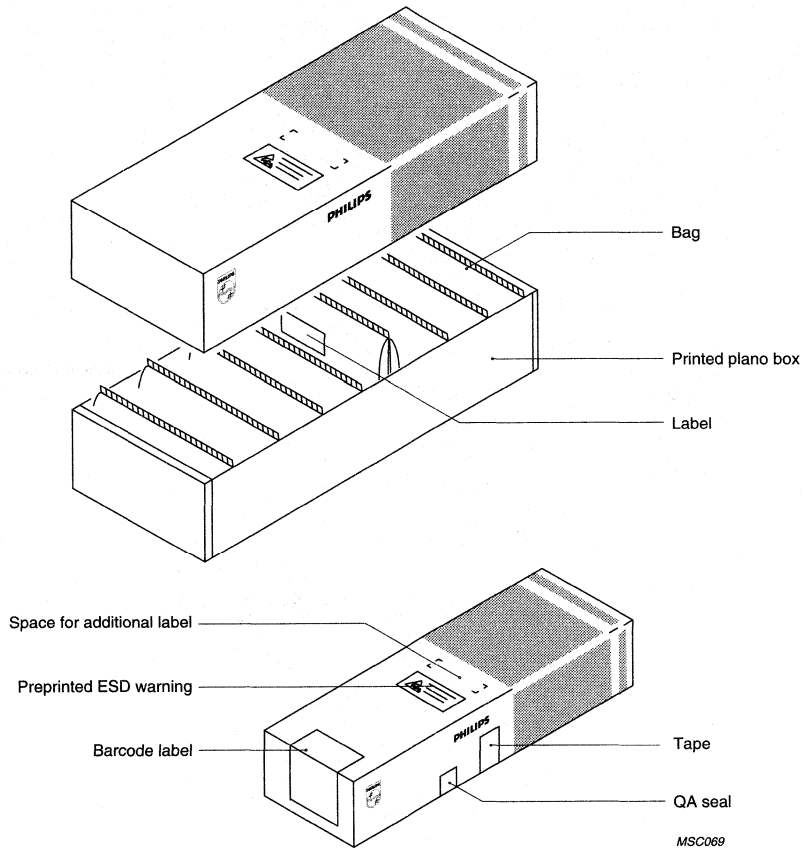
Fig.9 Tube pack.

Packing Methods

Chapter 6

Item	Material	Weight <sup>(1)</sup> (g)
Printed plano box	Cardboard carbon coated	125.00
Tape	Polypropylene	0.10
Labels	Paper	2.00
Bag	Polyethylene	12.00
Seal	Acrylate	0.15

<sup>(1)</sup> For SOT54



MSC069

Fig.10 Bulk pack (bag).

## Packing Methods

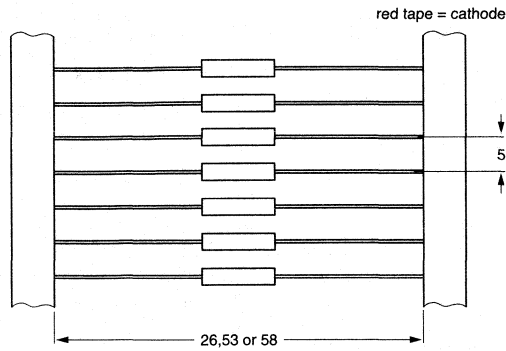
## Chapter 6

**PACKING QUANTITIES, BOX DIMENSIONS AND CARRIER SHAPES****Reel pack - axial and radial taped**

<b>PHILIPS PACKAGE TYPE/OUTLINE CODE</b>	<b>WIDTH (mm)</b>	<b>METHOD</b>	<b>SPQ</b>	<b>PQ</b>	<b>OUTER BOX DIMENSIONS L × W × H (mm)</b>
<b>SOD</b>					
SOD27	26	axial	10000	10000	358 × 358 × 56
SOD27	52	axial	10000	10000	356 × 356 × 88
SOD27	37	radial	5000	5000	360 × 360 × 60
SOD51	52	axial	5000	5000	356 × 356 × 88
SOD53	37	radial	2000	10000	395 × 395 × 290
SOD57	52	axial	5000	5000	356 × 356 × 88
SOD57	52	axial	10000	10000	356 × 356 × 88
SOD61	52	axial	5000	5000	356 × 356 × 102
SOD64	52	axial	5000	5000	356 × 356 × 88
SOD66	52	axial	5000	5000	356 × 356 × 88
SOD68	26	axial	10000	10000	358 × 358 × 56
SOD68	52	axial	10000	10000	356 × 356 × 88
SOD81	52	axial	5000	5000	356 × 356 × 88
SOD83	52	axial	2000	2000	356 × 356 × 102
SOD84	52	axial	5000	5000	356 × 356 × 88
SOD88	52	axial	5000	5000	356 × 356 × 102
SOD89	52	axial	2000	2000	356 × 356 × 102
SOD91	52	axial	10000	10000	356 × 356 × 88
<b>SOT</b>					
SOT54	32	radial	2000	10000	395 × 395 × 290

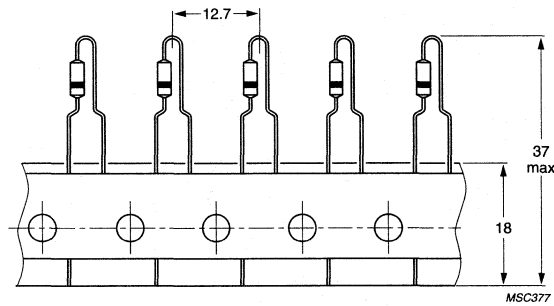
Packing Methods

Chapter 6



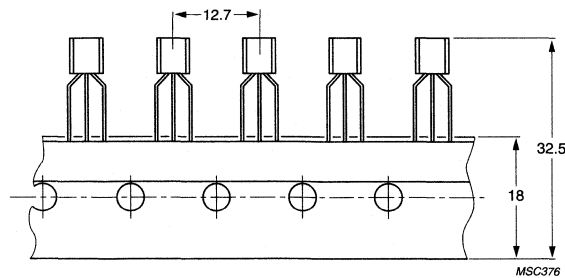
MSC081

Fig.11 Axial taped components for reel pack.



MSC377

Fig.12 Radial taped components for reel pack.



MSC376

Fig.13 Radial taped components for reel pack.

## Packing Methods

## Chapter 6

## Tape and reel - surface mount devices

PHILIPS PACKAGE TYPE/OUTLINE CODE	REEL DIMENSIONS D × W (mm)	SPQ AND PQ	REELS PER BOX	OUTER BOX DIMENSIONS L × W × H (mm)
<b>SOT</b>				
SOT23	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT89	180 × 12	1000	1	186 × 186 × 24
	330 × 12	4000	1	338 × 338 × 24
SOT143	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT173	180 × 16	600	1	186 × 186 × 24
SOT223	180 × 12	1000	1	186 × 186 × 24
	330 × 12	4000	1	338 × 338 × 24
SOT323	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT343	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT346	180 × 8	3000	1	186 × 186 × 16
SOT353	180 × 8	3000	1	186 × 186 × 16
SOT363	180 × 8	3000	1	186 × 186 × 16
SOT404	330 × 24	800	1	340 × 340 × 38
<b>SOD</b>				
SOD80	180 × 8	2500	1	186 × 186 × 16
	330 × 8	10000	1	338 × 338 × 18
	330 × 8	50000	5	339 × 339 × 71
SOD87	180 × 8	2000	1	186 × 186 × 16
	180 × 8	10000	5	182 × 182 × 55
	330 × 8	8000	1	338 × 338 × 18
	330 × 8	40000	5	339 × 339 × 71
SOD106	180 × 12	1500	1	186 × 186 × 24
SOD110	180 × 8	3000	1	186 × 186 × 16
	330 × 8	10000	1	338 × 338 × 18
SOD123	180 × 8	3000	1	186 × 186 × 16
	330 × 8	10000	1	338 × 338 × 18
SOD323	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18



## Packing Methods

## Chapter 6

## Tape and reel - surface mount devices

PHILIPS PACKAGE TYPE/OUTLINE CODE	CARRIER TAPE DIMENSIONS (mm) (See Figs. 14 and 15)				
	A0	B0	K0	P1	W
<b>SOT</b>					
SOT23	3.1	2.6	1.3	4.0	8.0
SOT89	4.3	4.6	1.6	8.0	12.0
SOT143	3.1	2.6	1.3	4.0	8.0
SOT173	8.5	8.5	1.8	12.0	16.0
SOT223	7.0	7.4	1.9	8.0	12.0
SOT323	2.4	2.4	1.2	4.0	8.0
SOT343	2.4	2.4	1.2	4.0	8.0
SOT346	3.1	3.2	1.3	4.0	8.0
SOT353	2.4	2.4	1.2	4.0	8.0
SOT363	2.4	2.4	1.2	4.0	8.0
SOT404	10.6	15.8	4.9	16	24.0
<b>SOD</b>					
SOD80	1.6	3.9	1.7	4.0	8.0
SOD87	2.0	3.9	2.3	4.0	8.0
SOD106	3.1	5.6	2.7	4.0	12.0
SOD110	1.6	2.3	1.6	4.0	8.0
SOD123	1.6	4.0	1.2	4.0	8.0
SOD323	1.6	2.9	1.2	4.0	8.0

Packing Methods

Chapter 6

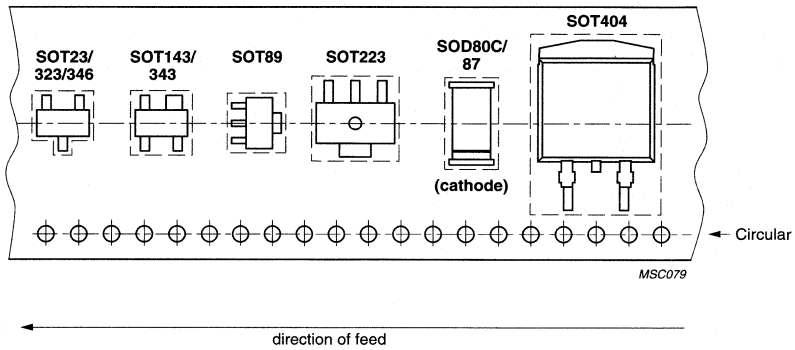


Fig.14 Product orientation in carrier tape for surface mount devices.

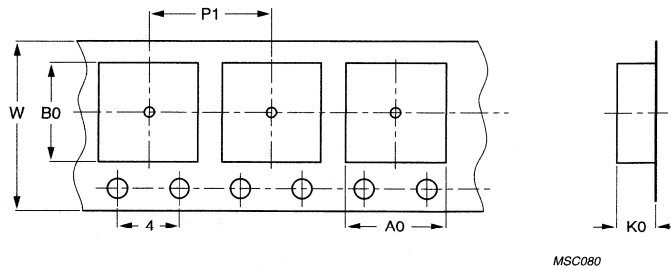


Fig.15 Carrier tape for surface mount devices.

## Packing Methods

## Chapter 6

## Ammo pack - axial and radial taped

PHILIPS PACKAGE TYPE/OUTLINE CODE	TAPE WIDTH (mm)	TAPING METHOD	SPQ/PQ	OUTER BOX DIMENSIONS L × W × H (mm)
SOD27	26	axial	5000	263 × 48 × 75
SOD27	52	axial/small	1000	138 × 73 × 29
SOD27	52	axial	10000	263 × 74 × 124
SOD27	37	radial	5000	350 × 203 × 42
SOD57	52	axial/small	200	138 × 73 × 29
SOD57	52	axial	2500	263 × 73 × 87
SOD61	52	axial	500	305 × 118 × 65
SOD61	52	axial/small	50	138 × 73 × 29
SOD64	52	axial	2500	263 × 73 × 87
SOD64	52	axial/small	200	138 × 73 × 29
SOD66	52	axial	5000	263 × 73 × 122
SOD66	52	axial/small	1000	138 × 73 × 29
SOD68	26	axial	5000	263 × 48 × 75
SOD68	52	axial/small	1000	138 × 73 × 29
SOD68	52	axial	10000	263 × 73 × 124
SOD68	37	radial	5000	350 × 203 × 42
SOD68	52	axial/small	500	138 × 73 × 29
SOD81	26	axial	5000	255 × 50 × 89
SOD81	52	axial	5000	263 × 73 × 87
SOD81	52	axial/small	500	138 × 73 × 29
SOD84	52	axial	2500	263 × 73 × 87
SOD84	52	axial/small	200	138 × 73 × 29
SOD91	52	axial/small	1000	138 × 73 × 29
SOD91	52	axial	2000	263 × 73 × 102
SOD91	26	axial	5000	263 × 48 × 75
SOD91	52	axial	10000	253 × 74 × 124

Packing Methods

Chapter 6

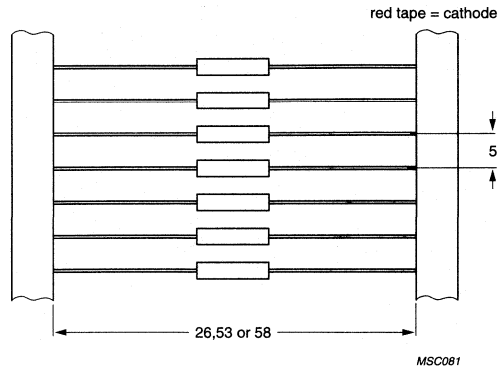


Fig.16 Axial taped components for ammo pack.

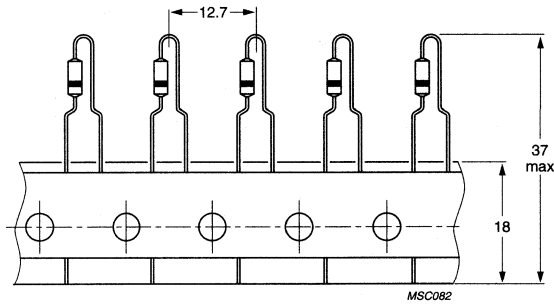


Fig.17 Radial taped components for ammo pack.

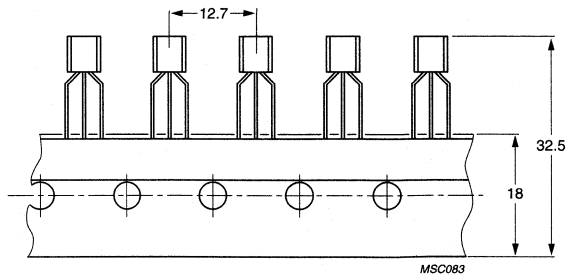


Fig.18 Radial taped components for ammo pack.

## Packing Methods

## Chapter 6

## Blister pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER CARRIER <sup>(1)</sup>	CARRIER PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	PACKING VERSION (See Fig.19)
SOT48	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT48	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT55	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT55	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT56	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT56	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT115	25 (12 + 13)	4	100	315 × 118 × 78	B
SOT115	5 (1 × 5)	1	5	145 × 100 × 29	C
SOT119	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT119	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT120	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT120	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT121	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT121	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT122	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT122	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT123	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT123	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT130	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT130	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT132	12 (3 × 4)	5	60	315 × 118 × 78	A
SOT132	12 (3 × 4)	3	36	315 × 118 × 78	B
SOT147	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT147	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT160	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT160	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT161	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT161	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT171	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT171	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT172	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT172	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT179	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT179	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT181	30 (3 × 10)	5	150	315 × 118 × 78	A
SOT183	15 (3 × 5)	5	75	315 × 118 × 78	A
SOT233	15 (3 × 5)	5	75	315 × 118 × 78	A
SOT246	15 (3 × 5)	5	75	315 × 118 × 78	A

## Packing Methods

## Chapter 6

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER CARRIER <sup>(1)</sup>	CARRIER PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	PACKING VERSION (See Fig.19)
SOT262	20 (2 × 10)	3	60	315 × 118 × 78	B
SOT262	4 (1 × 4)	8	32	315 × 118 × 78	D
SOT268	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT268	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT273	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT273	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT278	12 (3 × 4)	5	60	315 × 118 × 78	A
SOT279	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT279	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT288	15 (3 × 5)	5	75	315 × 118 × 78	A
SOT289	20 (2 × 7 + 1 × 6)	2	40	315 × 118 × 78	B
SOT289	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT321	45 (3 × 15)	11	495	315 × 118 × 78	A
SOT321	45 (3 × 15)	1	45	145 × 100 × 29	C
SOT324	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT324	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT342	30 (2 × 15)	8	240	315 × 118 × 78	A
SOT347	16 (2 × 8)	3	48	315 × 118 × 78	B
SOT350	20 (2 × 10)	5	100	315 × 118 × 78	A
SOT359	60 (5 × 12)	9	540	315 × 118 × 78	A
SOT365	15 (3 × 5)	5	75	315 × 118 × 78	A
SOT390	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT390	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT391	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT391	4 (2 × 2)	8	32	315 × 118 × 78	D
SOT406	16 (2 × 8)	5	90	315 × 118 × 78	A
SOT437	20 (2 × 7 + 1 × 6)	3	60	315 × 118 × 78	B
SOT437	4 (2 × 2)	8	32	315 × 118 × 78	D
CATV+C	2 (1 × 2)	1	2	315 × 118 × 78	B
CR2424	25 (5 × 5)	4	100	315 × 118 × 78	B
BGY887	1 (1 × 1)	1	4	145 × 100 × 29	C
CR2427	21 (3 × 7)	3	63	315 × 118 × 78	B
CATV	25 (12 + 13)	4	100	315 × 118 × 78	B

**Note**

1. SPQ is given with the packing method in parenthesis. For example:
  - a) 20 (2 × 10) means an SPQ of 20 pieces, packed in 2 rows of 10 pieces.
  - b) 20 (2 × 7 + 1 × 6) means an SPQ of 20 pieces, packed in 2 rows of 7 pieces plus 1 row of 6 pieces.

# Packing Methods

# Chapter 6

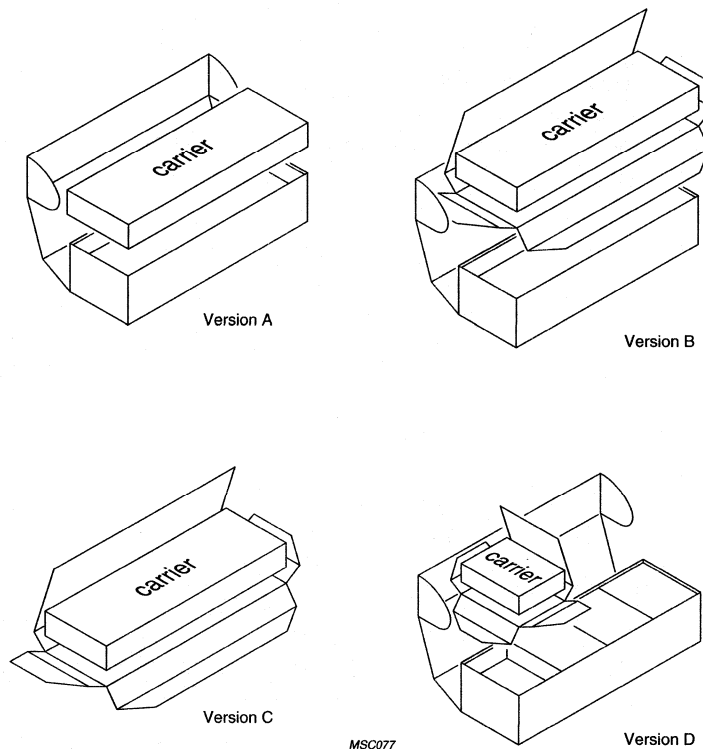
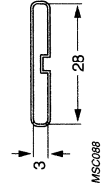
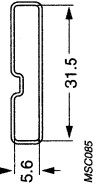
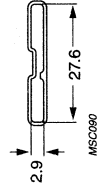
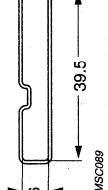
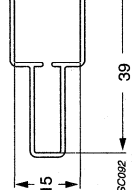
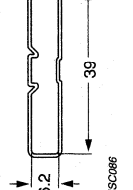


Fig.19 Packing versions of blister pack.

## Packing Methods

## Chapter 6

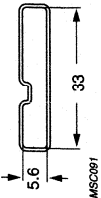
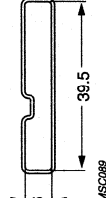
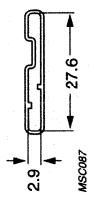
Tube pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	CARRIER LENGTH (mm)	END STOP	SPQ	CARRIERS PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	CARRIER PROFILE
SOT32	390	turnlock	50	20	1000	402 × 95 × 29	
SOT263	520	turnlock	50	20	1000	526 × 69 × 75	
SOT78	520	turnlock	50	20	1000	526 × 69 × 75	
SOT82	390	turnlock	50	20	1000	402 × 95 × 29	
SOT93	396	turnlock	25	20	500	408 × 86 × 81	
SOT199 bent lead	396	turnlock	25	12	300	408 × 86 × 81	
SOT93 bent lead	396	turnlock	25	12	300	408 × 86 × 81	
SOT128	523	endstop	50	20	1000	529 × 84 × 85	



## Packing Methods

## Chapter 6

PHILIPS PACKAGE TYPE/OUTLINE CODE	CARRIER LENGTH (mm)	END STOP	SPQ	CARRIERS PER BOX	PQ	OUTER BOX DIMENSIONS L x W x H (mm)	CARRIER PROFILE
SOT186	520	turnlock	50	20	1000	526 x 69 x 75	 MSC081
SOT199	396	turnlock	25	20	500	408 x 86 x 81	 MSC089
SOT399	413	turnlock	25	20	500	425 x 107 x 87	 MSC087

# Packing Methods

# Chapter 6

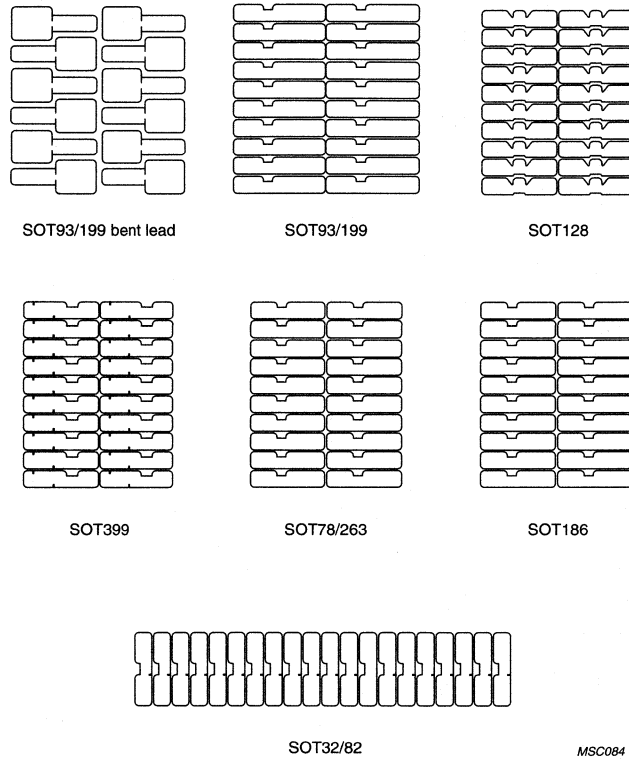


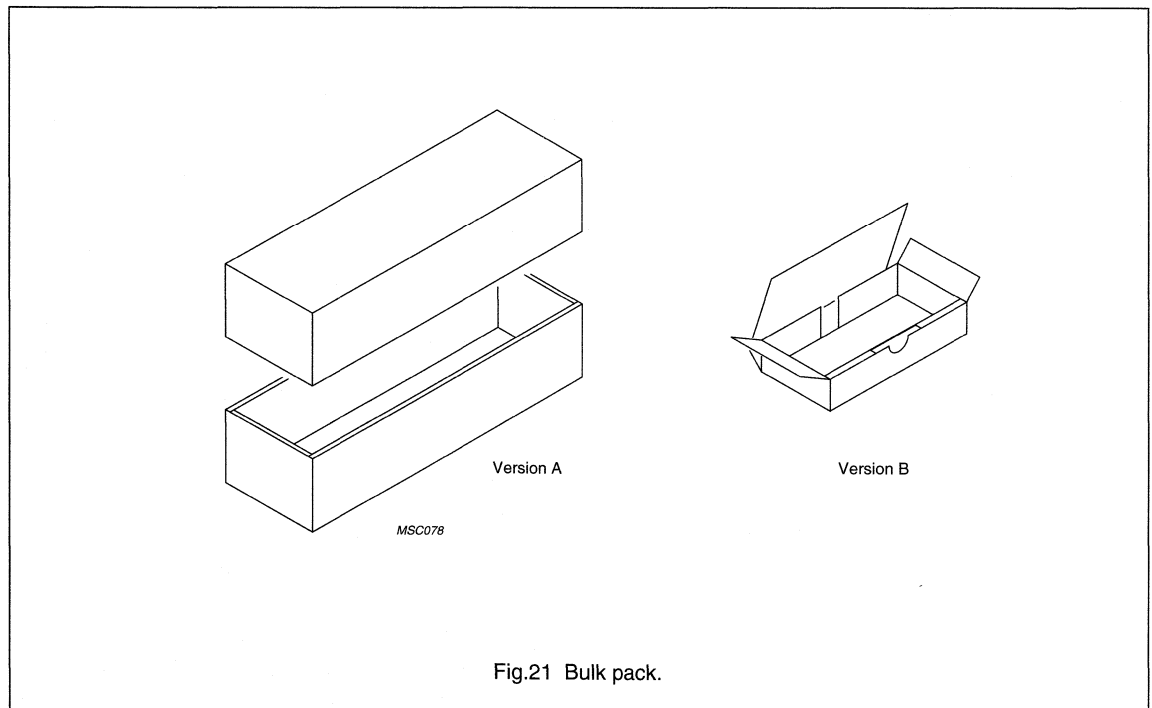
Fig.20 Stacking method tubes.

## Packing Methods

## Chapter 6

## Bulk pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER BAG	BAGS PER BOX	PQ	PACKING VERSION (See Fig.21)	OUTER BOX DIMENSIONS L × W × H (mm)
<b>SOT</b>					
SOT5	50	20	1000	A	315 × 115 × 75
SOT18	1000	5	5000	A	315 × 115 × 75
SOT18	250	16	4000	A	315 × 115 × 75
SOT37	500	18	9000	A	315 × 115 × 75
SOT54	500	8	4000	A	315 × 115 × 75
SOT89	250	80	20000	A	315 × 115 × 75
SOT223	250	80	20000	A	315 × 115 × 75
<b>SOD</b>					
SOD57	100	15	1500	A	315 × 115 × 75
SOD57	250	1	250	B	138 × 73 × 30
SOD80	1000	10	10000	B	138 × 73 × 30
SOD87	1000	6	6000	B	138 × 73 × 30





## Chemical content of devices

## Chapter 7

### INTRODUCTION

Nowadays, everyone must accept responsibility for keeping the environment clean, from individuals adopting a responsible attitude to their own waste disposal, however small that may be, to big industries who must take proper precautions to avoid releasing large amounts of damaging waste into the environment.

As a leading electronic components manufacturer, Philips Semiconductors has always regarded environmental protection as a major issue. The electronics industry, like many others, produces its share of toxic and hazardous materials, and we have long made it our policy to follow working practices that cut the chance of these materials passing into the environment to the absolute minimum.

Products supplied by Philips Semiconductors today offer no hazard to the environment in normal operation and when stored according to the instructions given in our data sheets. Inevitably, some products contain substances that are potentially hazardous to health if exposed by accident or misuse, but we ensure that users of these components receive clear warning of this in the data sheets. And where necessary, the warning notices contain safety precautions and disposal instructions.

This chapter supplements these notices and instructions by providing clear and comprehensive information on the composition of representative examples of ICs manufactured by Philips Semiconductors. This information should form a basis for answering questions on product safety and disposal and should, moreover, help to increase awareness of these aspects, not only throughout the Philips Semiconductors organization but throughout the semiconductor industry in general.

### EXPLANATION OF THE TABLES

The following pages provide the chemical constituents of representative groups of discrete semiconductor components down to minor percentages and traces, as far as these constituents may be important to the use, destruction or disposal of the components.

The tables contain information about the materials used in the semiconductor devices themselves and in the packing used for storage, transport and assembly.

Whenever possible, the devices have been grouped into families based on the similarity in composition, construction and packing method. In this way we were able to limit the number of tables. For each group, one representative is specified in mass percentages of its parts.

In many cases, a single envelope type will contain a range of differing leadframes with different die-pad dimensions to accommodate the active devices. This, however, leads to only minor changes in the mass percentages. Different materials or techniques are sometimes used to assemble one envelope type, and whenever possible, alternative materials are included in the tables. In other cases only the standard or high-volume process is described.

Per page, the product family is defined and the types identified by the Philips package code number. Additionally, reference is made to usual names or to the JEDEC code (when applicable). The mass in grams (g), body dimensions in millimeters (mm) and packing quantity are also specified.

The table itself shows the composition of the group representative broken down into the device-parts:

- metal parts
- crystal
- envelope (plastic, glass or ceramic)
- packing materials

The device-parts are specified in milligrams (mg). These figures are as accurate as possible for the group representative shown. Other devices from the same group may differ considerably in mass. The amount of packing material, specified in grams, per device can be found by dividing the weight of the packing material by the packing quantity. For more detailed information on packing, refer to Chapter 7 Packing Methods.

### Metal parts

The composition of the leadframe material is indicated, when appropriate, by the method commonly used for alloys, e.g.:

- FeNi42 means iron alloy containing 42% of nickel (alloy 42).
- CuZn15 means copper alloy containing 15% zinc (tombac).
- Cu alloy indicates copper with a small amount of alloying elements such as Fe, Ni, Zn or Ag or combinations of some elements.

### Crystal

The active device is usually a silicon chip doped with very small amounts of elements such as boron, arsenic or phosphorus. The back may be metallized with thin layers of titanium, nickel, platinum, gold or silver to enhance die-bonding to the leadframe.

## Chemical content of devices

## Chapter 7

### Envelope

The chip is protected by a glass, ceramic, plastic or metal encapsulation.

Glass will contain  $\text{SiO}_2$  plus a number of oxides of Ba, K, Pb, Zn and Mn. These elements are, however, immobilized and will not be extracted by acids, unless the glass is ground.

The plastic encapsulation is usually based on ortho cresol novolac (OCN) -epoxy or on biphenyl-epoxy, filled with quartz particles (fused or crystalline) up to approximately 70 mass percent. In all cases (except SOT54), antimony trioxide and tetrabromobisphenol-A (TBBA) are present as flame retardants. The TBBA will be incorporated in the epoxy-polymer after curing so that no TBBA is present in the finished device. It has become a partially brominated epoxy. The flammability of all moulding compounds rates typically UL94-V0 at 1/8 inch.

### Packing material

Cardboard and paper consist mainly of natural fibres. The carbon layer for ESD protection does not hamper the recyclability of the cardboard.

Polyethylene, polypropylene and polystyrene are synthetic polymers made from hydrocarbons.

Polyvinylchloride (PVC), a synthetic polymer made from chlorinated hydrocarbons, is used for the tubes in which many semiconductors are packed. PVC is hazardous to the environment when burned under certain, ill-controlled conditions. PVC is, however, readily recyclable when the material is collected separately (as a mono-material).

Therefore the endpins, turnlocks and soft rubber stoppers in the PVC-tubes are now replaced by PVC to enhance recycling.

The re-use of the polystyrene (PS) reels is encouraged by requesting all our customers to return the reels after use to Semi-cycle. Information and addresses are printed on the boxes in which the reels are delivered. Philips Semiconductors' intention is to buy used reels, when available, thus closing the product life circle to lower the amount of wasted packing materials.

To encourage recycling, Philips Semiconductors marks the packing materials according to ISO 11469 using the recycling symbols shown in Figs 1 to 1. Figure 1 shows the symbol for paper and cardboard, Figs 2 to 1 show the symbols for various plastics.



Fig.1 Paper and cardboard.



Fig.2 Polyethylene terephthalate.

## Chemical content of devices

## Chapter 7



Fig.3 Polyethylene, high density.

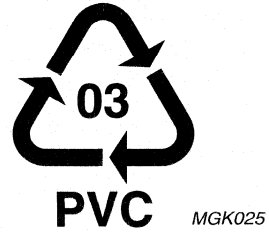


Fig.4 Polyvinylchloride.



Fig.5 Polyethylene, low density.



Fig.6 Polypropylene.

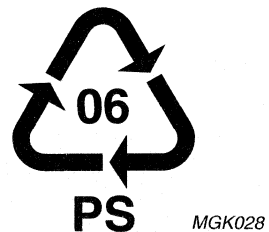


Fig.7 Polystyrene.



Fig.8 Other plastics. The acronym of the plastic is put under the recycling symbol. In this example: PA = polyamide.

## Chemical content of devices

## Chapter 7

**SUBSTANCES NOT USED BY PHILIPS SEMICONDUCTORS**

Below are listed the materials and substances that are **not** present in Philips Semiconductors' products and processes. This information supplements the chemical contents tables that follow and is provided to enable equipment manufacturers to make a complete and confident assessment of the environmental impact of selecting products manufactured by Philips Semiconductors.

**Substances not used in products**

- 4-aminodiphenyl and its salts
- ammonium salts
- arsenic
- asbestos
- benzene
- cadmium and compounds
- creosote
- cyanates
- cyanides
- 4,4-diaminophenyl methane
- dibenzofurans
- epichlorhydrine
- ethylene glycol ethers
- formaldehyde
- halogenated aliphatic hydrocarbons
- hydrazine
- mercury and compounds
- N-nitrosoamines
- 2-naphthylamine and its salts
- nickel tetracarbonyl
- N,N-dimethylformamide
- N,N-dimethylacetamide
- oils and greases
- organometallic compounds (e.g. org. tin compounds)
- ozone-depleting compounds
- pentachlorophenol
- phenol compounds
- (nonyl)-phenol ethoxylates
- phtalates
- picric acid
- polybrominated biphenyl oxides (PBBO)
- polybrominated biphenyls (PBB/PBBE)
- polychlorinated triphenyls (PCT)
- polychlorinated naphthalenes
- polychlorinated biphenyls (PCB)
- polycyclic compounds
- polyhalogenated dibenzofurans/dioxins
- polyhalogenated bi/triphenyl ethers
- selenium
- tellurium
- tetrabromobenzylimidazole
- tetrabromoethylene
- toluene
- triethylamine
- tris (aziridinyl) phosphinoxide
- tris (2,3-dibromopropyl) phosphate
- vinyl chloride monomer
- xylene

**Substances not used in manufacturing processes**

Philips Semiconductors has eliminated all Ozone Depleting Substances, referred to as Class I and II in the Montreal Protocol and its amendments. This means that our products, in compliance with the US Clean Air Act, do not have to be labelled.

We have also eliminated, voluntarily, the use of chlorinated hydrocarbons such as perchloro-ethylene and trichloro-ethylene from our manufacturing processes.

Below is a summary of the ozone-depleting substances we have eliminated.

## Class I substances:

- fully halogenated chloro-fluorocarbons (CFC)
- halons
- carbontetrachloride
- 1,1,1-trichloroethane

## Class II substances:

- partially halogenated hydrocarbons (HCFC)

**Substances not used in packing materials**

- laminates with paper
- bleached paper
- polystyrene flakes (EPS)



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## Chemical content of devices

## Chapter 7

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### DISPOSAL

Old or used products must be disposed of in accordance to national and local regulations.

The products and packing materials must be disposed of as special waste. This is required, in particular, for parts containing environmentally hazardous materials, for example beryllium oxide, present in some RF-devices.

Smaller quantities of material may be disposed of as domestic waste, provided national or local regulations permit this.

### RECYCLING

Where legally required, we accept packing materials and products for recycling and/or disposal. However, since the cost of returning these materials to us must be borne by the customers, it is often more cost effective for them to look for a local recycle company. To assist in this we can provide customers with the names and addresses of local recycle companies in their areas.

### GENERAL WARNINGS

#### Products

Under the specified operating conditions, no hazardous materials will be liberated from the products. The general warnings describe phenomena that can be expected with

**abnormal** use (outside the product's specification). For example:

- If a product is exposed to strong acids, metals contained within it may be partially extracted.
- If a product with an epoxy moulded envelope is exposed to organic solvents, these may extract part of the resin contained in the envelope.
- If the product is incinerated, degradation and condensation reactions in the organic material it contains may cause a number of hazardous substances to be released into the air in unpredictable amounts. Moreover, metal oxides will be formed and may be released into the air as dust particles.
- If products with beryllium heatsinks (RF transistors) are damaged, toxic beryllium oxide dust may be released into the air.

#### Packing material

- With adequate oxygen supply, packing materials will give off mainly carbon dioxide and water if burned. However, if they are burned in a limited oxygen supply (the general case in a fire), hazardous compounds (for example carbon monoxide) may be emitted.
- PVC will form hydrochloric acid gas when incinerated. It will also generate a number of other chlorine compounds, among them the toxic dioxin, when the conditions (temperature, oxygen) are not well controlled.

## Chemical content of devices

## Chapter 7

## GLASS DIODES/RECTIFIERS, LEADED

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
DO-35	SOD27	0.140	φ 1.9 × 4.3	5000
DO-41	SOD66	0.342	φ 2.6 × 4.8	5000
DO-34	SOD68	0.123	φ 1.6 × 3.0	5000
IT <sup>(2)</sup>	SOD81	0.283	φ 2.2 × 3.8	5000
IT <sup>(2)</sup>	SOD84	0.360	φ 3.2 × 4.3	5000
IT <sup>(2)</sup>	SOD91	0.123	φ 1.7 × 3.0	5000

## Notes

- All packages have a similar composition, quantities may vary.
- IT = implosion technology.

## Chemical content

DEVICE PART

Group representative: SOD68

DEVICE PART	SUBSTANCE	MASS (mg)
stud	FeNi42 cladded with Cu <sup>(1)</sup>	10.5
wire	Fe cladded with Cu	88
	plated with SnPb20	9
active device	doped Si	0.4
encapsulation	glass (Pb < 54%, Sb < 0.5%)	15
paint/pigment	epoxy copolymer	0.1

## Note

- Mo studs for implosion types.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	paper	53
tape	kraft paper	20
tape	polypropylene	19.6
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

**GLASS DIODES/RECTIFIERS, SMD**

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOD80	0.033	φ 1.5 × 3.5	2500
IT <sup>(2)</sup>	SOD87	0.053	φ 2.1 × 3.5	2500

**Notes**

1. All packages have a similar composition, quantities may vary.
2. IT = implosion technology.

**Chemical content**

DEVICE PART

Group representative: SOD87

DEVICE PART	SUBSTANCE	MASS (mg)
stud	Mo <sup>(1)</sup>	19.5
flange	Cu	15.0
	plated with SnPb20	2.5
active device	doped Si	0.4
encapsulation	glass (Pb < 54%, Sb < 0.5%)	15
paint/pigment	epoxy copolymer	0.1

**Note**

1. SOD80: FeNi42 clad with Cu.

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	39
carrier tape	polycarbonate, carbon loaded	18.8
cover tape	polyester	3.3

## Chemical content of devices

## Chapter 7

## GLASS-BEAD RECTIFIERS AND STACKS

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOD57	0.366	φ 3.8 × 4.6	2500
EHT-stack	SOD61	0.250	φ 3.0 × 12.5 max. <sup>(2)</sup>	5000
–	SOD64	0.840	φ 4.5 × 5.0	4000
EHT-stack	SOD83	1.015	φ 4.5 × 12.5 max. <sup>(2)</sup>	2000
EHT-stack	SOD88	0.360	φ 3.8 × 12.5 max. <sup>(2)</sup>	5000
EHT-stack	SOD89	1.210	φ 5.5 × 12.5 max. <sup>(2)</sup>	2000

## Notes

- All packages have a similar composition, quantities may vary.
- Body length depends on reverse voltage and may be less than given here.

## Chemical content

DEVICE PART

Group representative: SOD57

DEVICE PART	SUBSTANCE	MASS (mg)
stud	Mo	36
wire	Fe clad with Cu	198
	plated with SnPb20	5
active device	doped Si	3 <sup>(1)</sup>
encapsulation	glass (Pb < 6%)	124

## Note

- May be greater for EHT stacks.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	paper	53
reel	paper	25
tape	kraft paper	30
label	paper	0.8
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

**SMALL SIGNAL CERAMIC DIODE, SMD**

REFERENCE	PACKAGE CODE	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOD110	0.010	2.0 × 1.25 × 1.45	3000

**Chemical content**

DEVICE PART

Group representative: SOD110

DEVICE PART	SUBSTANCE	MASS (mg)
envelope	Al <sub>2</sub> O <sub>3</sub> , SiO <sub>2</sub>	8.2
	plated with Cu+SnPb20	1
encapsulation	OCN-epoxy polymer (SiO <sub>2</sub> < 70%)	0.8
active device	doped Si	<0.1

## PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	74
carrier tape	polycarbonate, carbon loaded	22.6
cover tape	polyester	4
labels	paper	2.1
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

## FLANGE-MOUNTED CERAMIC RF POWER TRANSISTORS

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT119	5.20	13.0 × 25.2 × 7.5	40
–	SOT121	5.00	13.0 × 25.2 × 7.5	40
–	SOT123	3.90	9.8 × 25.2 × 7.5	40
–	SOT160	4.86	9.8 × 25.2 × 7.5	75
–	SOT161	3.50	10.2 × 25.2 × 7.5	40
–	SOT171	3.60	5.9 × 25.2 × 7.0	40
–	SOT179	9.80	13.2 × 28.1 × 5.1	40
–	SOT262	8.00	10.4 × 34.3 × 5.8	16
–	SOT273	6.90	10.4 × 25.0 × 7.2	60
–	SOT289	8.20	11.8 × 28.1 × 4.6	40
–	SOT324	3.58	6.4 × 19.0 × 4.5	31

**Note**

1. All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOD119

DEVICE PART	SUBSTANCE	MASS (mg)
flange	Cu <sup>(1)</sup>	4120
leadframe	FeNi42 <sup>(2)</sup>	270
brazing alloy	AgCu28	20
encapsulation	Al <sub>2</sub> O <sub>3</sub>	200
heat spreader	BeO, plated with Mo/Ni/Au	540
active device	doped Si	10
glue	polyamide	40

**Notes**

1. In some types: WCu15 flange.
2. In SOT119A1 and SOT289: FeNiCo leadframe.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

## STUD-MOUNTED CERAMIC RF POWER TRANSISTORS

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT120A	3.00	φ 9.8 × 18.8	40
–	SOT122A	1.90	φ 7.6 × 17.0	40
–	SOT122C	1.50	φ 7.6 × 7.0	40
–	SOT147	11.40	φ 13.0 × 20.9	40
–	SOT172A	1.40	φ 5.4 × 16.0	40

**Note**

- All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOD122A

DEVICE PART	SUBSTANCE	MASS (mg)
stud <sup>(1)</sup>	Cu	800
leadframe	FeNi42 <sup>(2)</sup>	150
nut	CuZn37, plated with Ni	630
brazing alloy	AgCu28	30
encapsulation	Al <sub>2</sub> O <sub>3</sub>	120
heat spreader	BeO, plated with Mo/Ni/Au	120
active device	doped Si	10
glue	polyamide	40

**Notes**

- SOT122C: disk instead of a stud.
- SOT122A2: FeNiCo leadframe.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

## CERAMIC RF POWER TRANSISTORS IN PILL PACKAGE

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT119D	1.60	φ 13.0 × 4.5	40
–	SOT122D	0.70	φ 7.6 × 4.1	40
–	SOT172D	0.30	φ 5.4 × 3.6	40

**Note**

1. Ceramic packages without flange or stud (so called "pill"-packages) have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOD119D

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	FeNi42 <sup>(1)</sup>	370
brazing alloy	AgCu28	30
encapsulation	Al <sub>2</sub> O <sub>3</sub>	320
heat spreader	BeO, plated with Mo/Ni/Au	850
active device	doped Si	10
glue	polyamide	20

**Note**

1. FeNiCo in SOT119A1 and SOT289.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2



## Chemical content of devices

## Chapter 7

## FLANGE-MOUNTED RF POWER TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT48	4.00	φ 9.8 × 5.8	40
–	SOT55	13.40	φ 16.1 × 8.5	40
–	SOT56	5.40	φ 9.7 × 5.8	40

**Note**

1. All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOD48

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	FeNi42 <sup>(1)</sup>	670
nut	CuZn37, plated with Ni <sup>(1)</sup>	2225
brazing alloy	AgCu28	50
encapsulation <sup>(2)</sup>	OCN-epoxy polymer (SiO <sub>2</sub> < 72%, Sb < 3%, Br < 1%)	670
heat spreader	BeO, plated with Mo/Ni/Au	365
active device	doped Si	20

**Notes**

1. SOT55: Ni leadframe and nut.
2. SOT55: FeNiCo dome and glass encapsulation.

PACKING MATERIAL (TRAY PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	paper	50
sleeve	paper	19
plate/holder	paper	25
labels	paper	0.9

## Chemical content of devices

## Chapter 7

## POWER TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-220	SOT78	1.950	10.3 × 9.9 × 4.5	1000
–	SOT82	0.750	11.1 × 7.8 × 2.8	1000
–	SOT93	4.930	15.2 × 12.7 × 4.6	500
–	SOT186	1.950	10.2 × 9.5 × 4.6	1000
–	SOT186A	2.500	10.3 × 9.4 × 4.6	1000
–	SOT199	5.500	15.3 × 21.5 × 5.2	500
D2-pack	SOT404	1.700	10.3 × 9.5 × 4.5	800

**Note**

1. All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOD93

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu	3950
	plated with SnPb30	20
solder pellet	SnAg25Sb10 <sup>(1)</sup>	25
encapsulation	OCN-epoxy polymer (SiO <sub>2</sub> < 72%, Sb < 3%, Br < 1%)	920
active device	doped Si	15

**Note**

1. Optional: PbSn5 solder pellet.

PACKING MATERIAL (TUBE PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	123
tubes	polyvinylchloride	700
turn locks	polyvinylchloride	20
labels	paper	15
tape	polypropylene	0.6
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

**MEDIUM-POWER TRANSISTORS IN PLASTIC PACKAGE**

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-126	SOT32	0.694	11.1 × 7.8 × 2.8	1000
TO-202	SOT128	1.528	11.1 × 7.8 × 2.7	1000

**Note**

1. All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOT128

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu, plated with Co /Au	863
	plated with SnPb30	15
active device	doped Si	10
encapsulation	silicon plastic	640

PACKING MATERIAL (TUBE PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	123
tubes	polyvinylchloride	836
end stops	polyvinylchloride	38
labels	paper	15
tape	polypropylene	0.6
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

## SMALL-SIGNAL TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-92	SOT54	0.250	$\phi$ 4.8 × 5.2	2000

## Chemical content

DEVICE PART

Group representative: SOT54

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	CuZn15, plated with Co/Au	113
	plated with SnPb30	1.5
active device	doped Si	0.5
encapsulation <sup>(1)</sup>	OCN-epoxy polymer (SiO <sub>2</sub> < 72%, Sb < 4%, Br < 0.6%)	135

## Note

- Alternative: two-shot encapsulation of epoxy and PPS.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	97.5
carrier tape	kraft paper	110
buffer	cardboard	20

## Chemical content of devices

## Chapter 7

## RF TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
T-pack	SOT37	0.115	φ 4.8 × 2.7	9000
X-pack	SOT103	0.122	φ 4.8 × 2.7	5000

## Note

1. All packages have a similar composition, quantities may vary.

## Chemical content

## DEVICE PART

Group representative: SOT37

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	CuZn15, plated with Co/Au	30
	plated with SnPb30	0.6
active device	doped Si	0.5
encapsulation	OCN-epoxy polymer (SiO <sub>2</sub> < 72%, Sb < 4%, Br < 0.6%)	84

## PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	125
bag	polyethylene	52
label	paper	1.4

## Chemical content of devices

## Chapter 7

**TRANSISTORS IN METAL PACKAGE**

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-39	SOT5	0.97	$\phi$ 8.5 × 6.6	1000
TO-18	SOT18	0.31	$\phi$ 4.8 × 5.3	5000

**Note**

1. All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOT18

DEVICE PART	SUBSTANCE	MASS (mg)
metal envelope + leads	FeNi28Co18	240
wires + solder	Au	2
solder layer	Sn	5
part of encapsulation	glass	62
active device	doped Si	1

PACKING MATERIAL (BULK PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	125.4
bag	polyethylene	14.5
label	paper	1.4

## Chemical content of devices

## Chapter 7

## TRANSISTORS AND DIODES IN PLASTIC PACKAGE, SMD

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOD106	75	4.7 × 2.5 × 2.6	1500
–	SOD123	7	2.7 × 1.5 × 1.1	3000
–	SOD323	4	1.7 × 1.3 × 0.9	3000
–	SOT23	8	2.9 × 1.3 × 0.9	3000
–	SOT89	50	4.5 × 2.5 × 1.5	1000
–	SOT143	8	2.9 × 1.3 × 0.9	3000
–	SOT223	126	6.5 × 3.5 × 1.6	1000
SC70-3	SOT323	5	2.0 × 1.3 × 0.9	3000
–	SOT343	6	2.0 × 1.3 × 0.9	3000
SC70-5	SOT353	5	2.0 × 1.3 × 0.9	3000
SC70-6	SOT363	5	2.0 × 1.3 × 0.9	3000

**Note**

- All packages have a similar composition, quantities may vary.

**Chemical content**

DEVICE PART

Group representative: SOT23

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	FeNi42 <sup>(1)</sup>	2.6
	plated with SnPb20	0.3
active device	doped Si	0.1
encapsulation	OCN-epoxy polymer (SiO <sub>2</sub> < 72%, Sb < 2%, Br < 1%)	5.0

**Note**

- Optional: copper-plated NiFe leadframe.

PACKING MATERIAL (BULK PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	74
carrier tape	polycarbonate, carbon loaded	22.6
cover tape	polyester	4
labels	paper	2.1
seal	acrylate	0.2

## Chemical content of devices

## Chapter 7

## RF-MODULES

REFERENCE	PACKAGE CODE <sup>(1)</sup>	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT132	34.7	67.5 × 19.7 × 8.1	36
–	SOT246	12.0	45.0 × 14.2 × 6.3	75
–	SOT278	19.6	60.5 × 11.0 × 7.0	150
–	SOT321	2.6	24.8 × 13.2 × 4.0	150
–	SOT342	3.5	36.5 × 11.5 × 3.8	100
–	SOT347	16.5	36.0 × 25.0 × 18.0	48
–	SOT348	10.0	27.2 × 23.5 × 6.0	100
–	SOT350	5.1	34.5 × 12.0 × 4.0	100

## Note

- All packages have a similar composition, quantities may vary.

## Chemical content

DEVICE PART

Group representative: SOT278

DEVICE PART	SUBSTANCE	MASS (mg)
heatsink	Cu, plated with Ni/Au	12700
leads	CuSn8, plated with SnPb	200
solder	PbIn and SnAg	400
bond wires	Au	40
substrate	Al <sub>2</sub> O <sub>3</sub> , plated with Au/Pt/Ag/Pd	1250
active devices	doped Si, Au metal	60
surface-mount capacitors	BaTiO <sub>3</sub> , Ag	1200
surface-mount resistors	Al <sub>2</sub> O <sub>3</sub> , Ru, Ni, Sn	1200
cap	polyethylene terephthalate	1950
glue	silicon rubber	600

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box/plate	paper	112
blister	polystyrene	123.5
blister	styrene/butadiene copolymer	120
tape	polypropylene	0.8
seal	acrylate	0.2



## Chemical content of devices

## Chapter 7

## CATV-MODULE

REFERENCE	PACKAGE CODE	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT115	14.4	13.8 × 44.8 × 20.8	25

## Chemical content

DEVICE PART

Group representative: SOT115

DEVICE PART	SUBSTANCE	MASS (mg)
heatsink	Al, plated with Ni	8000
leads	CuSn8, plated with SnPb	200
solder	PbIn and SnAg	1000
bond wires	Au	60
alumina + thin film substrate	Al <sub>2</sub> O <sub>3</sub> + Au, Ni, Cr, Cu,	800
active devices	doped Si, Au metal	60
surface-mount capacitors	BaTiO <sub>3</sub> , Ag	1500
cap	PET	2200
glue	silicon rubber	600

## PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	21
blisters	polystyrene	17.5
label	paper	0.6
seal	acrylate	0.6

## Chemical content of devices

## Chapter 7

## PLASTIC LEADLESS MODULE CARRIER

REFERENCE	PACKAGE CODE	MASS (g)	BODY (mm)	PACKING QUANTITY
stick 3612	SOT385	0.42	12 × 6 × 3	5000
stick	SOT408	0.48	12 × 6 × 3.5	5000
coin	SOT412	4.60	φ 25.3 × 4.9	500

## Chemical content

DEVICE PART

Group representative: SOT412

DEVICE PART	SUBSTANCE	MASS (mg)
foil	epoxy polymer + metal pattern	80
coil	Cu	768
active device	doped Si	5
surface mounted capacitor	BaTiO <sub>3</sub> , Ag	52
encapsulation	OCN-epoxy polymer (SiO <sub>2</sub> < 70%, Sb < 4%, Br < 0.6%)	3700

PACKING MATERIAL (BULK PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	130
bags	polyethylene	5
label	paper	1.4

## Chapter 8

## Data handbook system

### DATA HANDBOOK SYSTEM

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IC27	Complex Programmable Logic Devices

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SC08b	RF Power Transistors for UHF
SC09	RF Power Modules and Transistors for Mobile Phones
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### Professional components

PC06	Circulators and Isolators
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## Chapter 8

## Data handbook system

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**Sweden:** STOCKHOLM, Tel. (+46) 8 632 2000, Fax. (+46) 8 632 2745.  
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For all other countries apply to:

**Philips Components,**  
 Marketing Communications,  
 P.O. Box 218,  
 5600 MD EINDHOVEN, The Netherlands  
 Fax. +31-40-2724547.



# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,  
Fax. +43 160 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
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**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoprojekt, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7318

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 0044

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
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**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd. Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO,  
Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA,  
Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo,  
SAO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI,  
Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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